16V, 25A Stackable Switching Buck Regulator Module

MCPF1525M06

Description

The MCPF1525M06 is a fully integrated, highly efficient, and user-friendly point-of-load voltage regulator module. It incorporates an on-chip pulse-width modulation (PWM) controller, integrated MOSFETs, and built-in inductors and capacitors, resulting in a compact and precise solution. Its low-profile package is optimized for automated assembly using standard surface-mount equipment. The MCPF1525M06 supports programmable operation via I^2C and PMBus™ protocols. Comprehensive development and optimization have resulted in the smallest, most efficient, and fully featured 25A–200A point-of-load solution available today. Integrated protection features include pre-biased start-up, soft-start protection, overvoltage protection, thermally compensated overcurrent protection with hiccup mode, and thermal shutdown with auto-recovery.

Features

- POL Module With Integrated Inductor
- Small 6.8 mm × 7.65 mm × 3.82 mm Size
- 25A Continuous Output Rating
- Can be Stacked to 8 Modules for 200A Output
- No External Compensation is Required
- Differential Remote Voltage Sensing
- Programmable Operation With I^2C and PMBus
- 4.5V to 16V Input Voltage Range
- Output Voltage up to 1.8V
- Enable Input, Can Implement Programmable Undervoltage Lockout
- Power Good Output
- −40°C to 125°C Operating Range
- Lead and Halogen Free
- REACH and RoHS Compliant

Applications

- Telecommunications and Networking
- Data Center
- Storage
- Industrial
- Distributed Point of Load
- Computing Peripherals

Typical Application Circuits

Figure 1. 25A Single Module

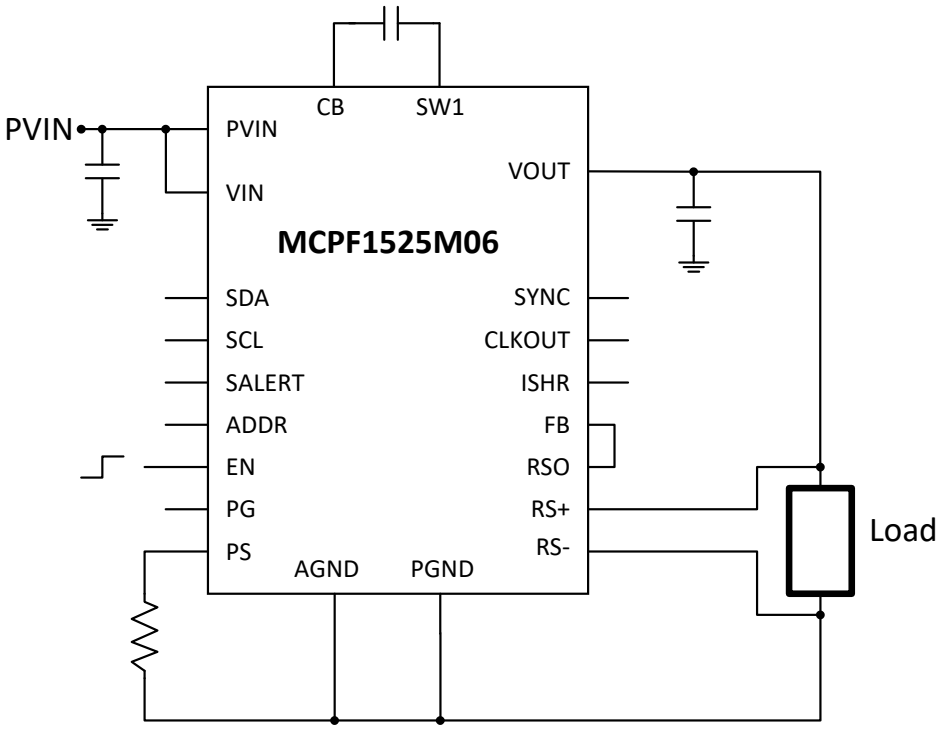
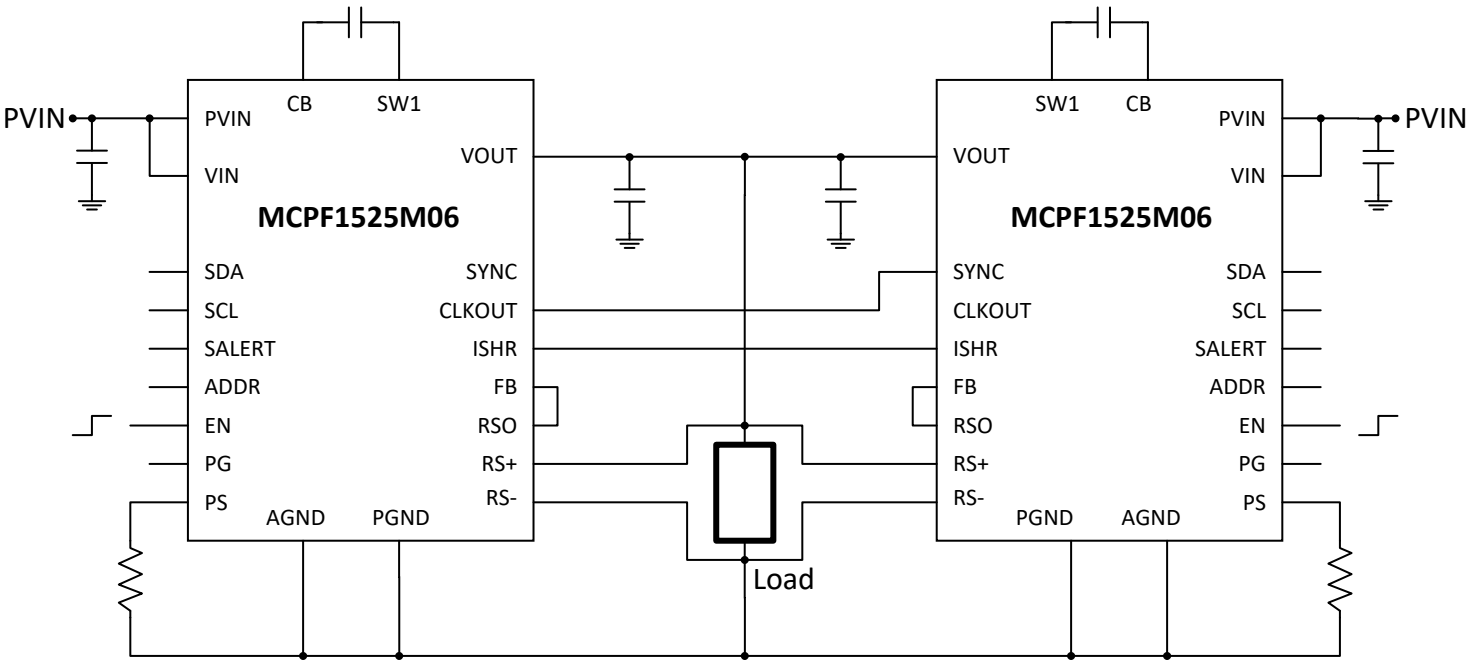
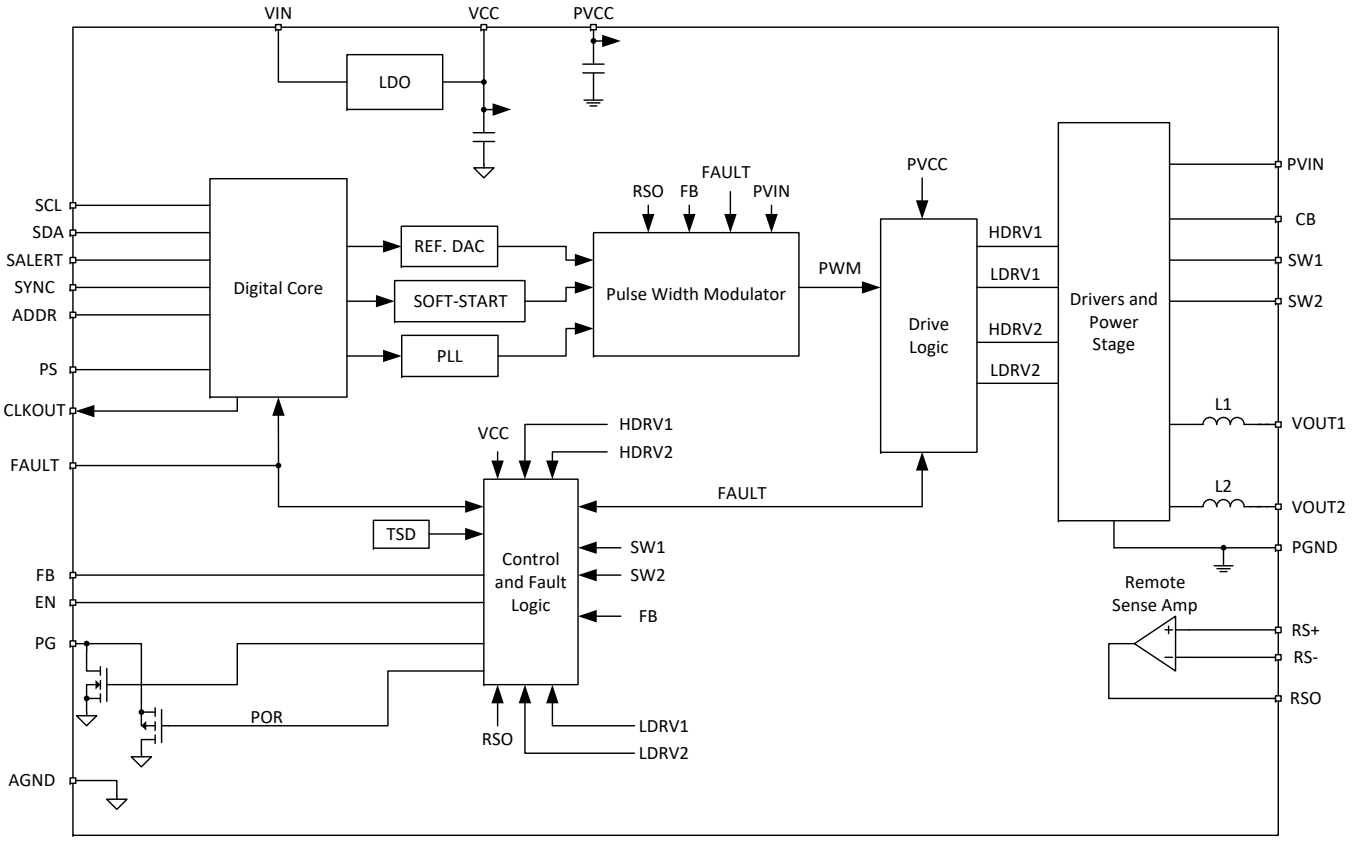


Figure 2. 50A, Two Stacked Modules



Block Diagram



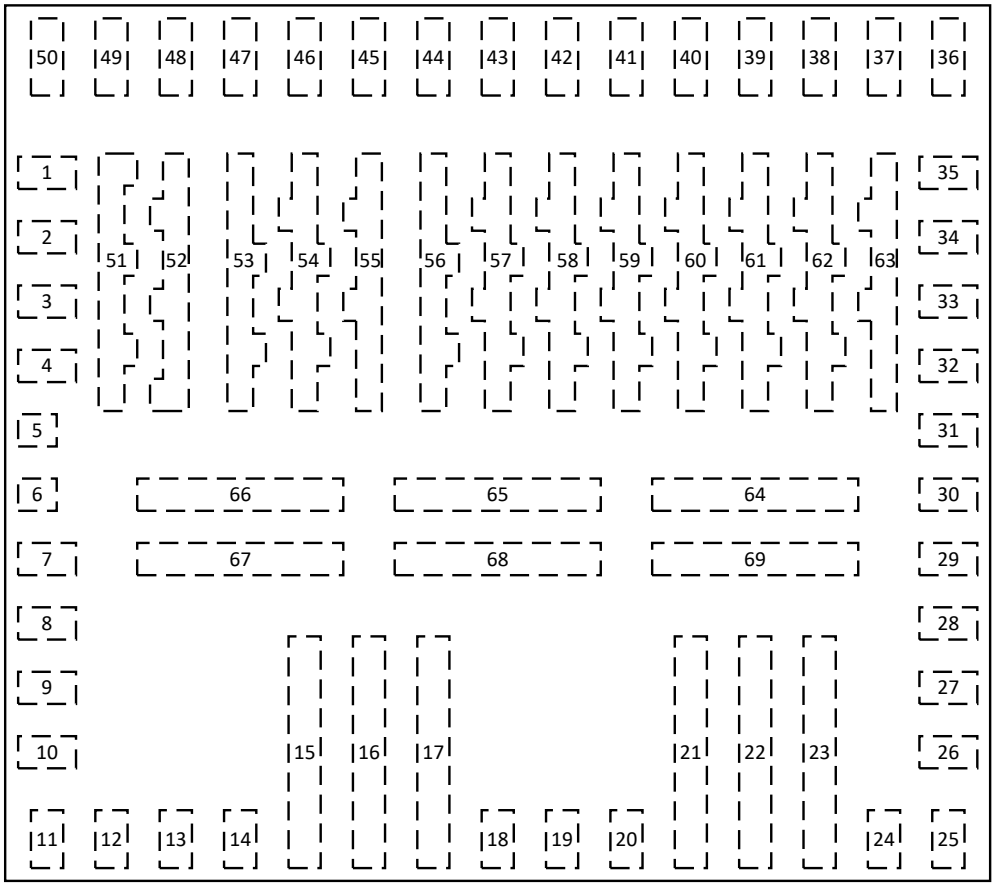
1. Pin Configuration

Pin Name	Pin Number	Pin Description
PVIN	1-4, 51, 52	Power input for the power stage driver circuits
BOOT1	5	Bootstrap pin for the phase 1 driver
BOOT2	6	Bootstrap pin for the phase 2 driver
SYNC	7	Synchronization clock input
VIN	8	Input supply for the internal LDO. Bypass with a 1 µF MLCC capacitor and connect to PVIN with a 2.7Ω resistor.
PVCC	9	Input supply for the drivers. Connect to VCC on the application board.
VCC	10	Output of the internal LDO. Can be used as an input for an externally applied bias. Bypass with a 1 µF MLCC capacitor and connect to the PVCC pin to supply the drivers. Input supply for the drivers.
PS	11	Phase setting selection pin. Connect a resistor from this pin to AGND to set the device as host or client as well as the number of devices connected in parallel to determine the relative phasing.
ADDR	12	Program the device address on the I^2C and PMBus using a resistor from this pin to AGND.
VFB	13	Feedback voltage for the device. Connect to RSO if the remote sensing amplifier is used. Otherwise, connect to the output voltage.
RSO	14	Output of the remote voltage sensing amplifier
VOUT2	15, 16, 17	Power output from phase 2 of the regulator. VOUT1 and VOUT2 should be shorted together and connected to the power output plane. Connect the output bypass capacitors from the power output plane to the power ground (PGND) plane.
RS+	18	Input of the remote differential sense amplifier. Connect this pin to the output voltage at the load.
RS-	19	Input of the remote differential sense amplifier. Connect this pin to ground at the load.
ISHARE	20	Current share bus pin.
VOUT1	21, 22, 23	Power output from phase 1 of the regulator. VOUT1 and VOUT2 should be shorted together and connected to the power output plane. Connect the output bypass capacitors from the power output plane to the power ground (PGND) plane.
FAULT#	24	Shares fault information with any parallel-connected devices. Active low. Must be pulled to VCC or another 5V source through a suitable resistance (5 kΩ) to allow device operation.
EN	25	Enable input used to turn the device on and off. It can be used to implement a UVLO function using an external resistor divider.
SCL	26	I^2C or PMBus clock line. Pull up to the bus rail using a 4.99 kΩ resistor.
SDA	27	I^2C or PMBus data line. Pull up to the bus rail using a 4.99 kΩ resistor.
SALERT	28	PMBus SMBALERT# line. Used to notify a host of an abnormal condition. Pull up to the bus rail using a 4.99 kΩ resistor.
CLKOUT	29	Phase-shifted clock output. For paralleled modules, connect this pin to the SYNC pin of the next part in the phase sequence.
PG	30	Open-drain power good output. Connect to VCC or an external bias using a resistor.
PGND	31-35, 56-63	Power ground for the power stage of the device. Connect to the output power ground plane.
SW1	36-43	Switched node of phase 1. Connect two 4.7 µF MLCC capacitors in parallel between this pin and CB.
NC	44	Not used, leave floating

Pin Configuration (continued)		
Pin Name	**Pin Number**	**Pin Description**
CB	45-50, 53-55	External flying capacitor connection. Connect two 4.7 µF MLCC capacitors between this pin and SW1.
AGND	64-69	Signal ground for the internal circuitry. Must be at least Kelvin-connected to the PGND net. Avoid routing that causes power currents to flow on this net.

1.1. Package Type

Figure 1-1. 8ZW Package, Top View



2. Functional Description

2.1. Overview

The MCPF1525M06 is a fully integrated, highly efficient, and user-friendly DC/DC regulator. Its output voltage and system optimization settings can be easily programmed via the I^2C/PMBus™ protocol. Featuring a proprietary modulator, the MCPF1525M06 delivers a rapid transient response. Internal stability compensation enables reliable operation across a wide range of applications and with different types of output capacitors, without concerns about loop stability.

This versatile device offers extensive flexibility for configuration and system monitoring through the I^2C and PMBus™ interfaces. Additionally, it supports standalone operation without a digital interface, allowing designers to set output voltages simply by adjusting resistor dividers and to monitor system status using the Power Good output.

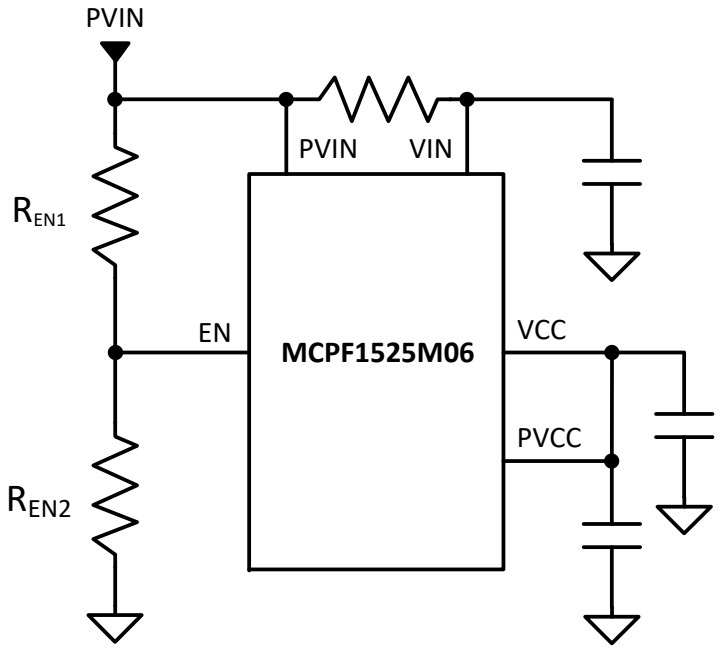
2.2. Operation and Topology

The MCPF1525M06 utilizes a modified interleaved buck converter topology that incorporates an coupling capacitor (CB) in the power path. This design reduces voltage stress on the internal power devices, allowing for smaller component sizes and lower switching losses than those of a conventional interleaved buck converter with the same rating. Additional benefits include a higher on-time, twice that of a standard buck converter for the same voltage conversion ratio, and inherent current sharing between the two phases, which is facilitated by the coupling capacitor.

2.3. Bias Voltage

The MCPF1525M06 features an integrated Low Drop-Out (LDO) regulator that supplies the DC bias voltage required for its internal circuits, typically providing an output of 5.2V. The input to this LDO is the VIN pin. For single-rail operation with internal bias, the VIN pin should be connected to the PVIN pin (see Figure 2-1). If an external bias voltage is preferred, connect the VIN pin to the VCC pin to bypass the internal LDO regulator (see Figure 2-2). A separate PVCC pin is provided to supply bias to the drivers, and this should be connected to VCC in the application circuit. It is recommended that VIN has a minimum slew rate of 0.06V/ms. Note that PVIN has internal undervoltage detection, which latches the device off if PVIN drops below 4.2V.

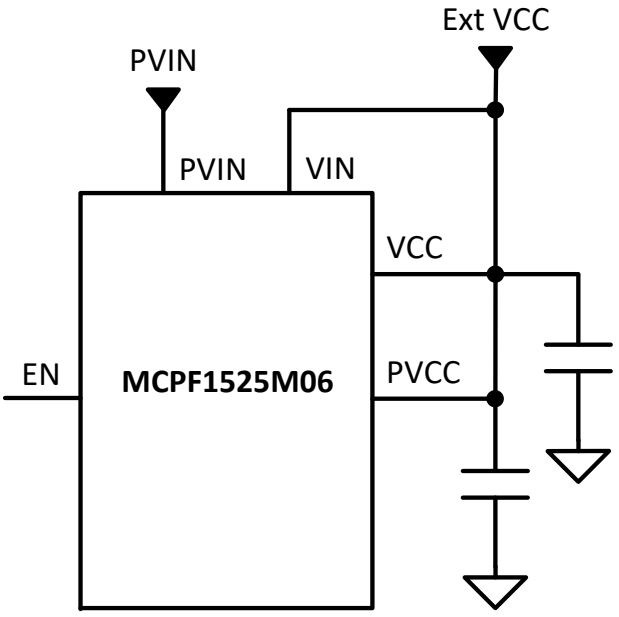
Figure 2-1. Using EN Pin as an Adjustable UVLO, Single Rail Operation Using Internal LDO



When using the EN pin as an adjustable UVLO, the threshold can be calculated as follows:

$$PVIN_{UV} = EN_{HIGH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}}$$

Figure 2-2. Using an External VCC Supply



The supply voltage—whether internal or external—ramps up with VIN and does not require activation via the EN pin. As a result, I²C/PMBus™ communication can begin as soon as the following conditions are met:

- The VCC_UVLO start threshold is reached
- Memory contents are loaded
- Initialization is complete
- The address offset is read

The I²C bus lines (SCL and SDA) must be pulled up to either VCC or the system I²C bus voltage with an external resistor. The MCPF1525M06 supports two selectable I²C bus voltage ranges, which can be set using the BUS_VOLTAGE_SEL bit in register 0x91:

Table 2-1. ISC Bus Voltage Control

Register	Bit	Name
0x91	[2]	BUS_VOLTAGE_SEL 0: 1.8V to 2.5V 1: 3.3V – 5V

2.4. I²C Base Address and Offsets

The MCPF1525M06 includes user-configurable registers for setting its I²C and PMBus™ base addresses. By default, the I²C base address is 0x10 and the PMBus™ base address is 0x70. An address offset ranging from 0 to 15 can be selected by connecting the ADDR pin to the AGND pin, either directly or through a resistor. During startup, an address detector measures the resistance of this connection to determine the offset value, which is then added to the base I²C address to establish the device's I²C communication address. The same offset is also applied to the base PMBus™ address to set the PMBus™ communication address.

To select offsets from 0 to 15, select the resistance from ADDR to AGND as follows:

Table 2-2. I²C/PMBus address offset resistors

Offset	Resistance (kΩ)
0	0
1	1.13
2	1.87
3	2.61
4	3.4
5	4.12
6	4.87
7	5.62
8	6.34
9	7.15
10	7.87
11	8.66
12	9.31
13	10.2
14	11
15	12.1

Note: Do not select the address 0x0C. This is the Alert Response Address used in the SMBus Alert Response Protocol.

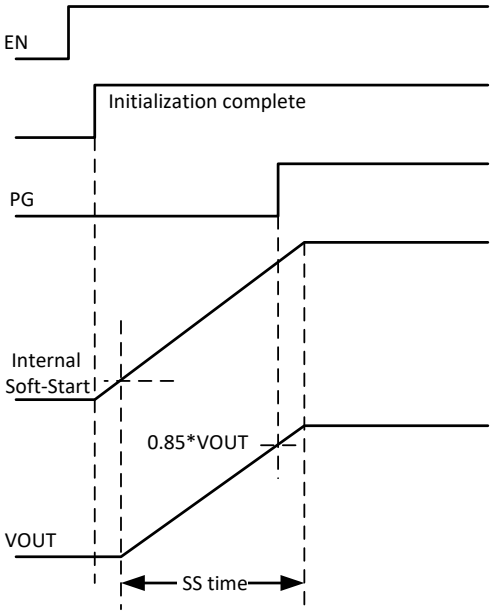
2.5. Soft-Start and Target Output Voltage

The MCPF1525M06 features an internal digital soft-start circuit that manages the output voltage ramp-up and limits inrush current during startup. When the startup conditions are satisfied, the soft-start process begins, ramping the output voltage toward the set reference at a rate specified by the TON_RISE registers (via the TON_RISE command), provided the following conditions are met:

- A valid enable signal is detected, as determined by the EN pin voltage, OPERATION register, and ON_OFF_CONFIG register.
- The input voltage PVIN is above the level set by PVIN UVLO threshold, which is set by the VIN_ON registers.
- The flying capacitor (CB) has been pre-charged to PVIN/2 by the internal pre-charge circuit, ensuring balanced PVIN/2 voltages across all FETs when switching begins.

During initial startup, the MCPF1525M06 uses minimum-width High-Drive (HDRV) pulses until the output voltage starts to rise (refer to the minimum on-time and off-time values in the electrical specifications). The on-time is gradually increased until VOUT reaches the target value set by the VOUT_COMMAND registers. While not strictly required, it is recommended to place a 100Ω resistor in parallel with the output capacitors (C_{OUT}) to ensure optimal startup performance.

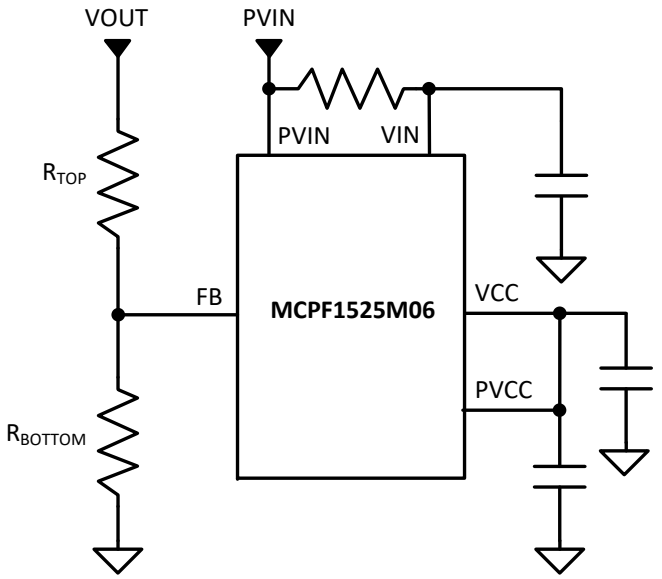
Figure 2-3. Operational Waveforms at Startup



Overcurrent Protection (OCP) and Overvoltage Protection (OVP) are active during soft-start to safeguard against short circuits and excessive voltage levels.

A resistor divider can be used with the MCPF1525M06 device to set the required output voltage (see Figure 2-4). This approach allows system designers to configure all power rails within the full output voltage range (0.6–1.8V) using just one device.

Figure 2-4. Using an External Voltage Divider to Set the Output Voltage



The following equation can be used to calculate the resistor values in the voltage divider:

$$VOUT = V_{FB} \times \left(1 + \frac{R_{TOP} + \frac{R_{TOP} \times R_{BOTTOM}}{47.5}}{R_{BOTTOM}}\right)$$

Where:

- VOUT is the desired output voltage
- V_{FB} is the voltage at the feedback pin, 600 mV for the MCPF1525M06
- R_{TOP} is the value in kΩ
- R_{BOTTOM} is the value in kΩ

It is recommended that R_{TOP} be 1 kΩ and that a 2.7 nF feed forward capacitor is placed in parallel with it.

Alternatively, the output voltage can be configured via the I²C/PMBus™ command VOUT_COMMAND or the corresponding registers, eliminating the need for an external resistor divider. The MCPF1525M06 supports this command with a resolution of 1/1024V, and a reference resolution of 5 mV. Additionally, the initial output voltage can be selected using the PS resistor, which allows the user to choose from one of eight pre-programmed user register pairs (see the Phase Setting Pin section for details).

2.6. Shutdown Mechanisms

The MCPF1525M06 offers two shutdown options:

- **Hard Shutdown or Load-Dependent Decay:**
  When a valid hard-disable signal is detected (as determined by the EN pin, OPERATION register, ON_OFF_CONFIG register, input voltage PV_{IN}, and the PV_{IN} UVLO threshold set by the VIN_ON registers), both drivers are immediately turned off and the soft-start signal is pulled down immediately.
- **Soft-Stop or Controlled Ramp-Down:**

When a valid soft-off request is received (as defined by the EN pin, OPERATION register, and ON_OFF_CONFIG register), there is a delay specified by the TOFF_DELAY registers. After this delay, the soft-start voltage ramps down to 0 over a period set by the TOFF_FALL registers. The drivers are disabled only once the SS signal reaches 0. Ramping the soft-start voltage down causes the output voltage to decrease smoothly to 0.

By default, the device is set to perform a hard shutdown. Shutdown triggered by PVIN is always executed as a hard shutdown.

2.7. Phase Setting Pin (PS)

The PS pin on the MCPF1525M06 serves multiple functions:

1. **Parallel Operation:**
   When using multiple MCPF1525M06 devices in parallel, the phase relationship between modules (and thus the total number of devices) can be set by connecting a specific resistor value from the PS pin to AGND. In this configuration, the PS pin is used to designate one module as the "host."
2. **Switching Frequency Selection:**
   Certain resistor values, as shown in Table 2-3 below, allow the PS pin to set the device's switching frequency. It is recommended to select the switching frequency based on the output voltage according to:
   $700\ \mathrm{kHz} \times V_{OUT} \leq f_{SW} \leq 1.1\ \mathrm{MHz} \times V_{OUT}$
3. **Initial Output Voltage Selection:**
   The PS resistor can also be used to set the initial output voltage at startup, according to the values in Table 2-3. Any subsequent output voltage changes made via PMBus commands will override this initial setting.

Table 2-3. PS Resistor Values and Functions

R_{PS}, kΩ	Host/Client	Phase degrees	Initial VOUT	F_{SW} (MHz)
0	Host	0	0.6	See Table 2-4
1.13	Client	180	0.6	Sync to host
1.87	Client	120	0.6	Sync to host
2.61	Client	90	0.6	Sync to host
3.4	Client	72	0.6	Sync to host
4.12	Client	60	0.6	Sync to host
4.87	Client	51.4	0.6	Sync to host
5.62	Client	45	0.6	Sync to host
6.34	Host	0	0.6	1.5
7.15	Host	0	1.2	1.25
7.87	Host	0	0.6	1.04
8.66	Host	0	0.6	0.892
9.31	Host	0	0.9	0.781
10.2	Host	0	0.85	0.694
11	Host	0	0.8	0.625
12.1	Host	0	0.7	0.568

The default voltage setting when operated in one of the host modes with R_{PS} 6.34 kΩ or greater can be programmed using registers 0x9D through 0xAC. These registers are in pairs for each setting, an upper byte and a lower byte. The high byte uses only bit [0] and the low byte uses bits [7:0] giving a 9 bit value. The default voltage can be calculated by:

$V_{BOOT} = value \times 5\ \mathrm{mV} + 500\ \mathrm{mV}$

Where:

- V_{BOOT} is the default boot up voltage
- *value* is the value in bits[8:0] in the upper and lower registers

Table 2-4. Switching Frequencies and Output Voltages

V_{OUT} range (V)	f_{SW} (MHz)
< 0.85V	0.625
0.85V < V_{OUT} < 1.1V	0.781
1.1V < V_{OUT} < 2.1V	1.25

2.8. Minimum Values for On-Time, Off-Time, and PVIN

When the input voltage (PV_{IN}) is much higher than the desired output voltage, the control MOSFETs are switched on for shorter durations. The shortest reliable on-time is defined by the minimum on-time (TON_{MIN}). During startup, when the output voltage is still low, the MCPF1525M06 operates at this minimum on-time.

The maximum conversion ratio is limited by two main factors:

1. **Minimum Off-Time ($TOFF_{MIN}$):**
   When the input voltage is close to the output voltage, the control MOSFET remains on for longer periods, and the minimum time it can be reliably turned off is defined by the minimum off-time ($TOFF_{MIN}$). During this interval, the synchronous MOSFET is on, and its current is monitored for overcurrent protection. This sets the lowest input voltage at which the device can still regulate the output to the target voltage.
2. **Phase Balance and Duty Cycle Limits:**
   To ensure balanced switching between both phases (or to keep the voltage on the CB pin at 0.5 × PV_{IN}), this topology requires that the high-side switches of the two phases do not overlap, unlike a conventional interleaved buck converter. This imposes a theoretical maximum duty cycle of 50% per phase and a maximum conversion ratio of 25%. In practice, accounting for circuit delays and dead times, the conversion ratio should not exceed 16% at full load.

Both system efficiency and load transient requirements can impact the maximum conversion ratio. It is recommended that system designers verify these values within their specific applications.

2.9. Enable (En) Pin

The Enable (EN) pin serves multiple purposes:

- **Primary On/Off Control:**

By default, as set by the ON_OFF_CONFIG command, the EN pin is used to turn the MCPF1525M06 on or off. It features a precise threshold that is monitored by the internal UVLO (Under-Voltage Lockout) circuit. If the pin is left unconnected, an internal 1 MΩ pull-down resistor ensures the MCPF1525M06 remains off to prevent accidental activation.

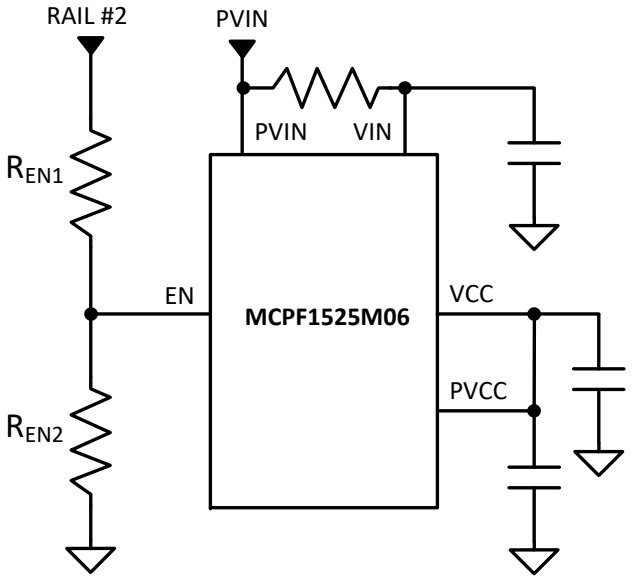
- **Input Voltage UVLO Implementation:**

The EN pin can be used to set an accurate input voltage UVLO threshold. Its input is derived from PVIN through external resistor dividers (R_{EN1} and R_{EN2}, see Figure 2-1). By adjusting these resistor values, users can program the UVLO threshold voltage, allowing for more precise control over PVIN UVLO levels than what is possible with the VIN_ON/VIN_OFF commands.

- **Power Sequencing:**

The EN pin can also be used to monitor other power rails, enabling specific power sequencing schemes (see the figure below).

Figure 2-5. Using EN to Monitor Another Rail



2.10. Overcurrent Protection (OCP)

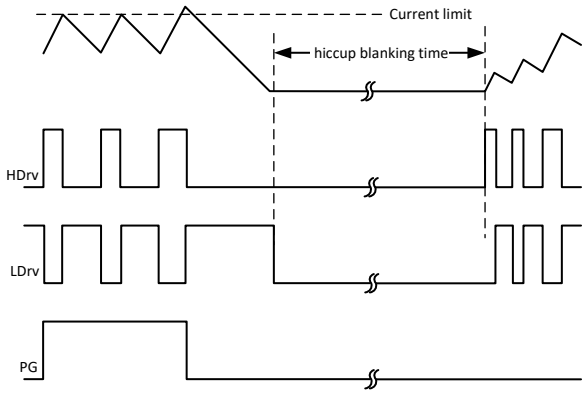
The MCPF1525M06 implements Overcurrent Protection (OCP) by monitoring the current through the $R_{DS(ON)}$ of the Synchronous MOSFET. If the sensed current exceeds the OCP threshold, a fault is triggered. This approach offers several advantages:

- Delivers accurate overcurrent protection without impacting converter efficiency, as the current sensing is lossless.
- Eliminates the need for a dedicated current-sense resistor, reducing cost.
- Minimizes layout-related noise issues.

The OCP threshold is set using the IOUT_OC_FAULT_LIMIT command or the corresponding user registers and can be programmed in 0.5A increments up to a maximum of 37.5A. The threshold is internally compensated to remain nearly constant across varying ambient temperatures.

When the current surpasses the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET stays on until the current drops to zero, after which the MCPF1525M06 enters hiccup mode (see Figure 2-6). During hiccup-blanking, both the Control and Synchronous MOSFETs remain off. After this period the MCPF1525M06 attempts to restart. If the overcurrent condition persists, the cycle repeats. The device will stay in hiccup mode until the fault is cleared. Alternatively, the MCPF1525M06 can be configured to enter a latched shutdown mode upon detecting an overcurrent fault using the IOUT_OC_FAULT_RESPONSE command or the corresponding register.

Figure 2-6. Hiccup Overcurrent Operation



2.11. Overvoltage Protection (OVP)

Overvoltage Protection (OVP) is implemented by monitoring the voltage at the FB pin. If the FB voltage exceeds the OVP threshold for longer than the specified OVP delay (typically 5 µs), a fault is triggered.

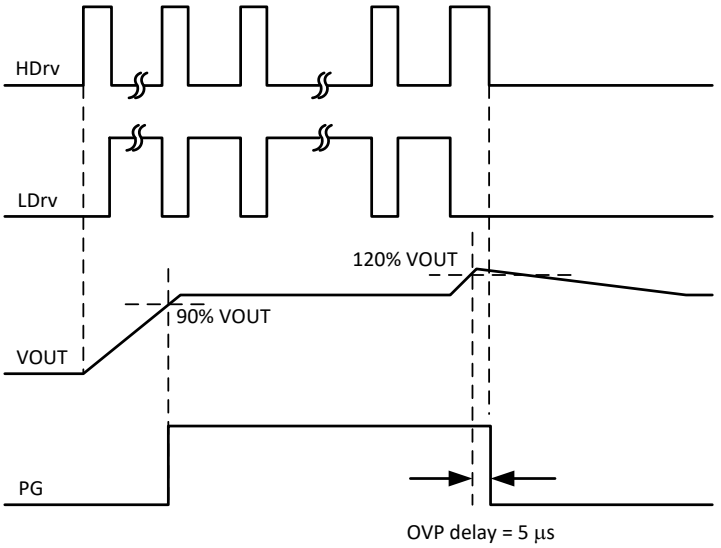
The OVP threshold is set using the VOUT_OV_FAULT_LIMIT command or the corresponding user registers. This command allows the overvoltage limit to be configured relative to the output voltage, with a resolution of 1/1024V. Internally, however, the threshold is rounded to one of four discrete settings, as detailed in the table below.

Table 2-5. VOUT_OV_FAULT_LIMIT Actual Values

VOUT_OV_FAULT_LIMIT (Relative to VOUT_COMMAND Value)	Actual OVP Threshold (Relative to VOUT_COMMAND Value)
100.0% < Setting ≤ 105.4%	105%
105.4% < Setting ≤110.1%	110%
110.1% < Setting ≤ 114.8%	115%
114.8% < Setting, or Setting ≤ 100%	120% (Default)

The default OVP threshold is set to 120%. When this limit is exceeded, all MOSFETs are immediately turned off and the PG pin is pulled low. The MOSFETs remain latched off until the fault is cleared by cycling either VCC or the EN pin. Figure 2-7 illustrates the timing sequence for overvoltage protection.

Figure 2-7. OVP Protection - Latched Response



The MCPF1525M06 offers output overvoltage and undervoltage warning features, as well as output undervoltage fault protection. These are configured using the VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, and VOUT_UV_FAULT_LIMIT commands (or their corresponding user registers). Unlike the overvoltage protection mechanism—which uses an all-analog signal path and a high-speed internal comparator—these warning and fault thresholds are determined by digitally comparing the processed VOUT telemetry data to the set limits.

2.12. Overtemperature Protection (OTP)

The MCPF1525M06 features internal temperature sensing, with a programmable threshold that can be set in 1°C increments using the OT_FAULT_LIMIT command (or the corresponding user registers). If this programmable threshold is set below the fixed analog limit of 145°C, it determines the trip point by digitally comparing the reported temperature (READ_TEMPERATURE) to the OT_FAULT_LIMIT value.

When the measured temperature exceeds the set threshold, the device will either continue normal operation (default) or enter a latched shutdown, depending on the configuration of the OT_FAULT_RESPONSE PMBus command (or the relevant registers). To recover from a latched shutdown, either the EN pin or OPERATION command must be cycled.

Additionally, an overtemperature warning threshold can be set using the OT_WARN_LIMIT command. This warning threshold is typically configured below the fault threshold and can be used to trigger an alarm via the PMBus™ ALERT pin and the STATUS_TEMPERATURE command.

2.13. Power Good (PG)

The behavior of the Power Good (PG) signal is determined by the user-configurable PGControl register bit and the POWER_GOOD_ON command. When PGControl is enabled, the PMBus™ command allows the upper power good threshold to be set relative to the output voltage, with a resolution of 1/1024V. Internally, however, this value is rounded to one of four discrete settings, as indicated in the table below.

Table 2-6. POWER_GOOD_ON Actual Values

POWER_GOOD_ON (Relative to VOUT_COMMAND Value)	Actual Threshold (Relative to VOUT_COMMAND Value)
95.1% < Threshold, or Threshold ≤ 79.6%	80%
79.6% < Threshold ≤ 85.1%	85% (Default)
85.1% < Threshold ≤ 89.8%	90%
89.8% < Threshold ≤ 95.1%	95%

The default setting is 85%, meaning the PG signal is asserted when the voltage at the FB pin rises above 85% of the VOUT_COMMAND value. The lower threshold is 5% below the upper threshold. If the voltage at the FB pin falls below this lower threshold, the PG signal is de-asserted (pulled low).

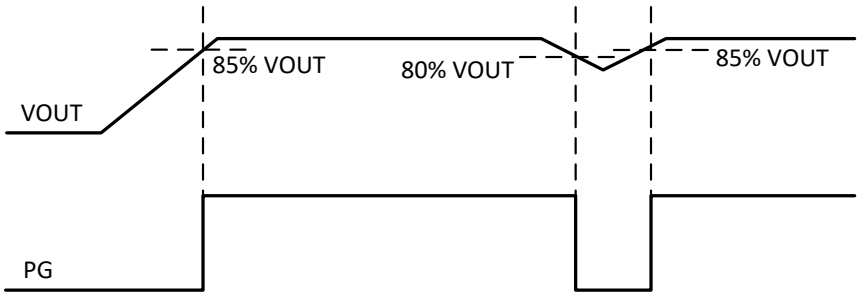
PGControl Bit Set to 1 (Default)

The PGControl bit is in register 0x91, bit[3]. There is no corresponding way to configure this using PMBus.

Table 2-7. PGControl Bit

Register	Bit	Name
0x91	[3]	PGControl 0: PG Based on PGOOD_ON_COMMAND 1: PG Based on DAC

Figure 2-8. PG Behavior With PGControl Set to 1



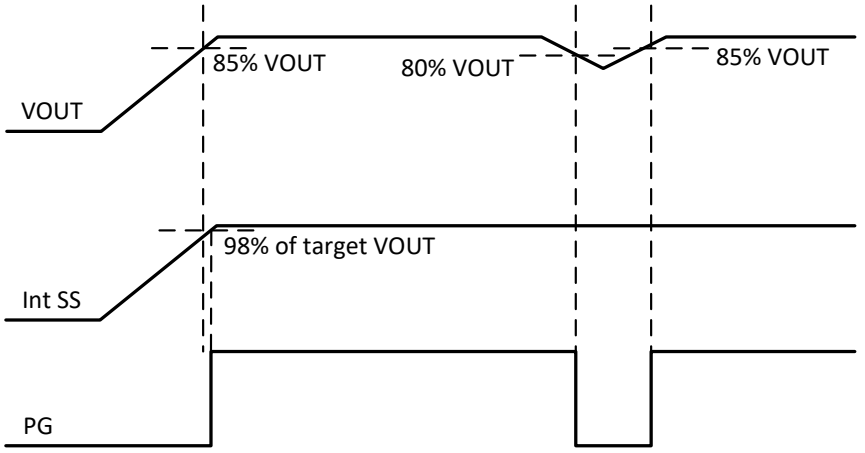
The behavior of the PG signal is consistent during both start-up and normal operation. The PG signal is asserted when all of the following conditions are met:

- Both EN and VCC are above their respective thresholds
- No faults are present (including overcurrent, overvoltage, or overtemperature)
- VOUT remains within the specified range (as determined by continuous monitoring of whether FB is above the PG threshold)

PGControl Bit Set to 0

The figure below shows PG behavior in this situation:

Figure 2-9. PG Behavior With PGControl Set to 0



During normal operation, the PG signal functions as it does when the PGControl bit is set to 1. However, at start-up, the PG signal is asserted once the FB pin is within 2% of the target output voltage, rather than when it exceeds the upper PG threshold.

Additionally, the MCPF1525M06 includes an internal PMOS transistor in parallel with the NMOS connected to the PG pin (see block diagram). This PMOS ensures that the PG signal remains at a logic low level even if VCC is low and the PG pin is pulled up to an external voltage different from VCC.

2.14. Remote Output Voltage Sensing (RS)

The MCPF1525M06 features high-performance true differential remote sensing to maintain output voltage accuracy by sensing the output voltage directly across the actual load, thereby compensating for voltage drops caused by high current. The remote sense amplifier is designed with a fast slew rate and both source and sink current capabilities, enabling it to respond quickly to output transients. This amplifier output is the source for the ADC that provides the data for the PMBus READ_VOUT command, and the registers VOUT_REPORT_LOWER (0xD6) and VOUT_REPORT_UPPER (0xD7). The resolution is 10 bits or 1/1024V.

2.15. Parallel Operation

MCPF1525M06 devices support parallel operation, allowing multiple units to be connected to the output voltage simultaneously and increasing load current capability. For all devices—including both host and client units—the RS+ pin should be tied to the output voltage, and the RS– pin should be connected to the ground reference.

For the host device, the RS+ and RS– inputs of the remote sense amplifier must be connected directly to the output voltage at the precise regulation point. This setup provides accurate feedback and compensates for voltage drops along the distribution path, ensuring optimal circuit performance.

Client devices are primarily responsible for current sharing, with voltage regulation being a secondary concern. Therefore, there is greater flexibility in how their RS+ and RS– pins are connected. While it is ideal to connect these pins to the same remote sense point as the host for consistency, this may not be practical due to the need for extensive PCB traces. In such cases, connecting the RS+ and RS– pins of client devices to the local output capacitors is recommended.

Device synchronization is achieved using the SYNC and CLKOUT pins, while the ISHARE pin facilitates current sharing among devices. The PS pin serves two purposes: on the host device, it sets the switching frequency; on client devices, it determines the phase relationship between the SYNC signal and the PWM clock, depending on the number of devices operating in parallel. This configuration enables interleaved operation with correct phase alignment for optimal system-level performance.

The MCPF1525M06 FAULT pin functions as both an input and output. It must be pulled up to VCC (or another 5V supply) for proper operation, even when only one device is used. In parallel configurations, the FAULT pin is essential for system protection, ensuring that a fault in any device is communicated to all others, causing them to shut down as well.

When operating modules in parallel, all must be configured identically for VOUT. There can be up to a 200 mV difference in the VOUT configuration between the host and client modules that is compensated for by the current share bus. Changing the output voltage in such a case can be done by first changing the host module and then changing the client modules in less than 200 mV increments. Changes larger than 200 mV can be made in successive steps.

2.16. Synchronization

If the device is synchronized to an external clock, the SYNC signal thresholds are 0.775 × VCC (high) and 0.45 × VCC (low). The clock frequency applied to the SYNC pin should be twice the desired PWM frequency, within the range of 568 kHz to 1.5 MHz.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter(s)	Symbol	Min.	Max.	Unit
PVIN, VIN, EN to PGND, CB to SW1		−0.3	18	V
VCC to PGND(1)		−0.3	6	V
SW1, SW2		−0.3	15	V
FB, PG and All Other I/O’s to AGND		−0.3	VCC	V
PGND to AGND(1)		−0.3	0.3	V
Moisture Sensitivity Level		MSL 3 JEDEC J-STD-020D		
ESD Classification		1.5 kV HBM JESD22-A114		

Note:

1. PGND and AGND must be connected together.

3.2. Recommended Operating Conditions

Parameter(s)	Symbol	Min.	Typ.	Max.	Unit
PVIN Range With External VCC(2)	PV_{IN}	$6*V_{OUT}$	—	16	V
PVIN Range With Internal LDO(3)	PV_{IN}, V_{IN}	$6*V_{OUT}$	—	16	V
Supply Voltage Range(1)	V_{CC}	4.5	—	5.5	V
Output Voltage Range	V_{OUT}	0.6	—	1.8	V
Continuous Output Current	I_O	0	—	25	A
Operating Junction Temperature	T_J	−40	—	125	°C

Notes:

1. Must not exceed 6V.
2. VIN is connected to VCC to bypass the internal LDO regulator.
3. VIN is connected to PVIN (single rail operations with PVIN = VIN = 4.5V to 5.5V).

3.3. DC/AC Characteristics

Unless otherwise stated, these specifications apply for: 6 × VOUT < PVIN < 16V, 4.5V < VIN < 16V, 0°C < T_J < 125°C						
Parameter(s)	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Current						
VIN Supply Current (Standby)	$I_{IN(STANDBY)}$	7	8.2	9.5	mA	EN low
VIN Supply Current (Static)	$I_{IN(STATIC)}$	8.8	10.5	12.2	mA	EN = 2V, no switching
VIN Supply Current (Dynamic)	$I_{IN(DYN)}$	47	51.5	56	mA	EN high, V_{IN} = 12V, F_{SW} = 625 kHz
Soft-Start						
Soft-start Time(1)	SS_{TIME}	2.3	3	3.7	ms	Default, V_{OUT} = 0.6V, T_{ON_RISE} = default setting
Output Voltage						
Output Voltage	V_{OUT}	—	0.6	—	V	Default
Output Voltage Range	V_{OUT}	0.6	—	1.8	V	

DC/AC Characteristics (continued)

Unless otherwise stated, these specifications apply for: 6 × VOUT < PVIN < 16V, 4.5V < VIN < 16V, 0°C < T_J < 125°C						
Parameter(s)	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
VOUT Resolution	V_{OUT}	—	5	—	mV	
VOUT Accuracy	V_{OUT}	−0.7	—	+0.7	%	T_J = 25 °C, V_{OUT} = 0.6V(3)
		−1.5	—	1.5	%	−40 °C ≤ T_J ≤ 105 °C, V_{OUT} = 0.6V(2, 3)
		−1	—	1	%	T_J = 25 °C, 0.6V ≤ V_{OUT} ≤ 1.8V(3)
ON Time						
ON Time	t_{ON}	155	180	205	ns	V_{IN} = 12V, V_{OUT} = 0.6V, F_{SW} = 625 kHz
Minimum ON Time(1)	$t_{ON(MIN)}$	—	50	—	ns	
Minimum OFF Time	$t_{OFF(MIN)}$	395	430	465	ns	T_J = 25 °C, F_{SW} = 625 kHz, PV_{IN} = 6V, V_{IN} = V_{CC} = PV_{CC} = 4.5V
Internal LDO Regulator						
Output Voltage	V_{CC}	4.9	5.2	5.4	V	5.5V < V_{IN} ≤ 16V, 0-75 mA
		4	—	—	V	4.5V < V_{IN} ≤ 5.5V, 0-55 mA
Line Regulation	V_{LN}	0	40	110	mV	5.5V < V_{IN} ≤ 16V, 0-75 mA
Load Regulation	V_{LD}	0	110	140	mV	0-75 mA
Short Circuit Current(1)	I_{SHORT}	130	151	172	mA	
Thermal Shutdown						
Threshold	T_{JSD}	—	145	—	°C	
Hysteresis		—	25	—	°C	
Undervoltage Lockout						
VCC Start Threshold	$VCC_{UVLO(STRT)}$	4.0	4.2	4.4	V	V_{CC} rising
VCC Stop Threshold	$VCC_{UVLO(STOP)}$	3.6	3.8	4.1	V	V_{CC} falling
EN Threshold Rising	EN_{HIGH}	1.14	1.2	1.36	V	EN rising
EN Threshold Falling	EN_{LOW}	0.9	1.0	1.06	V	EN falling
EN Input Impedance	R_{EN}	0.5	1.0	1.5	MΩ	
Current Limit						
Default Threshold	$I_{OC(def)}$	30.5	33	35.5	A	T_J = 25°C, V_{OUT} = 0.6V
Hiccup Time	t_{OC_HIC}	—	20	—	ms	
Overvoltage						
Default Threshold(1)	$V_{OVP(DEF)}$	110	120	130	%	
Delay Time	t_{OVPDLY}	—	5	—	µs	
Remote Sense Amplifier						
Differential Gain	A_{DIFF}	—	1	—	V/V	
Input Offset Voltage	V_{IOS}	—	0	—	mV	R_{SO} = 0.6V, no load
Output Sourcing Current	I_{SRC}	—	5.5	—	mA	RS+ = TBS, RS− = 0V, RSO = 1.8V
Output Sinking Current	I_{SNK}	—	0.55	—	mA	RS+ = 0V, RS− = −0.5V, RSO = 0.5V
Power Good						
Upper Threshold (Default)	$V_{PG(UP)}$	75	85	95	%	V_{OUT} rising
Hysteresis	$V_{PG(LOW)}$	—	5	—	%	V_{OUT} falling, differential to rising threshold
PG Sink Current	I_{PG}	6.6	8.8	11	mA	PG = 0.6V, EN = 2V
Telemetry						
PVIN Report Accuracy	$PVIN_{RPT\_ACC}$	−0.8	—	0.8	%	PV_{IN} = 12V, T_J = 25°C
		−1	—	1	%	PV_{IN} = 12V, −40°C ≤ T_J ≤ 125°C

DC/AC Characteristics (continued)						
Unless otherwise stated, these specifications apply for: 6 × VOUT < PVIN < 16V, 4.5V < VIN < 16V, 0°C < T_J < 125°C						
Parameter(s)	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
VOUT Report Accuracy	$VOUT_{RPT\_ACC}$	−2.5	—	2.5	%	V_{OUT} = FB = 0.6V, T_J = 25°C
		−3.2	—	3.2	%	V_{OUT} = FB = 0.6V, −40°C ≤ T_J ≤ 125°C
		−2	—	2	%	0.6V ≤ FB ≤ 1.8V, T_J = 25°C
		−2.5	—	2.5	%	0.6V ≤ FB ≤ 1.8V, −40°C < T_J < 125°C
IOUT Report Accuracy	$IOUT_{RPT\_ACC}$	0	—	2	A	PV_{IN} = 12V, T_J = 25°C, V_{OUT} = 0.6V, I_{OUT} = 0A
		0	—	2.5	A	PV_{IN} = 12V, −40°C ≤ T_J ≤ 125°C, V_{OUT} = 0.6V, I_{OUT} = 0A
Temperature Report Accuracy(1)	T_{RPT_ACC}	−10	—	10	°C	−40°C < T_J < 125°C

Notes:

1. Guaranteed by design, not production tested.
2. Performance over temperature guaranteed by correlation using statistical quality control but not tested in production.
3. Closed loop V_{OUT} measurement that includes all tolerances (reference, offsets, remote sense, switching ripple).

3.4. I²C Interface Electrical Characteristics

Unless otherwise stated, these specifications apply for: 6 × VOUT < PVIN < 16V, 4.5V < VIN < 16V, 0°C < T_J < 125°C, all parameters are guaranteed by design and are not production tested.							
Parameter	**Symbol**	**Fast Mode**		**Fast Mode Plus**		**Unit**	**Conditions**
I²C Paramters		**Min**	**Max**	**Min**	**Max**		
I²C Bus Voltage	V_{BUS}	1.8	5.5	1.8	5.5	V	
Low Level Input Voltage	V_{IL}	−0.5	$0.3V_{BUS}$	−0.5	$0.3V_{BUS}$	V	
High Level Input Voltage	V_{IH}	$0.7V_{BUS}$	—	$0.7V_{BUS}$		V	
Hysteresis	V_{HYS}	$0.05V_{BUS}$	—	$0.05V_{BUS}$		V	
Low Level Output Voltage 1	V_{OL1}	0	0.4	0	0.4	V	3 mA sink, V_{BUS} > 2V
Low Level Output Voltage 2	V_{OL2}	0	$0.2V_{BUS}$	0	$0.2V_{BUS}$	V	2 mA sink, V_{BUS} ≤ 2V
Low Level Output Current	I_{OL}	3	—	3	—	mA	V_{OL} = 0.4V
		6	—	6	—	mA	V_{OL} = 0.6V
Output Fall Time	t_{OF}	20 × (V_{BUS}/5.5V)	250	20 × (V_{BUS}/5.5V)	125	ns	V_{IHmin} to V_{ILmax}
Pulse Width of Spikes That Must be Suppressed	t_{SP}	0	50	0	50	ns	
Input Current I/O Pins	I_{IN}	−10	10	−10	10	µA	
Capacitance I/O Pins	C_{IN}	—	10	—	10	pF	
SCL Frequency	f_{SCL}	—	400	—	1000	kHz	
Hold Time (Repeated START)	t_{HD_ST}	0.6	—	0.26	—	µs	First SCL pulse after this time
SCL Low Time	t_{LOW}	1.3	—	0.5	—	µs	
SCL High Time	t_{HIGH}	0.6	—	0.26	—	µs	
Setup Time (Repeated START)	t_{SU_ST}	0.6	—	0.26	—	µs	

I2C Interface Electrical Characteristics (continued)							
Unless otherwise stated, these specifications apply for: 6 × VOUT < PVIN < 16V, 4.5V < VIN < 16V, 0°C < T_J < 125°C, all parameters are guaranteed by design and are not production tested.							
Parameter	Symbol	Fast Mode		Fast Mode Plus		Unit	Conditions
I^2C Paramters		Min	Max	Min	Max		
Data Hold Time	t_{HD_DAT}	0	—	0	—	µs	
Data Setup Time	t_{SU_DAT}	100	—	50	—	ns	
SDA, SCL Rise Time	t_R	20	300	—	120	ns	
SDA, SCL Fall Time	t_F	20 x (VCC/5.5V)	300	20 x (VCC/5.5V)	120	ns	
Setup Time for STOP Condition	T_{SU_STOP}	0.6	—	0.26	—	µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3	—	0.5	—	µs	
Capacitive Load on a Bus Line	C_B	—	400	—	550	pF	
Data Valid Time	t_{VD_DAT}	—	0.9	—	0.45	µs	
Data Valid ACK Time	t_{VD_ACK}	—	0.9	—	0.45	µs	
Noise Margin at Low Level	V_{NL}	$0.1V_{BUS}$	—	$0.1V_{BUS}$	—	V	Each device, including hysteresis
Noise Margin at Low Level	V_{NH}	$0.2V_{BUS}$	—	$0.2V_{BUS}$	—	V	
SDA Timeout	t_{TO}	200	—	200	—	µs	

Note:

1. Guaranteed by design, not production tested.

3.5. Thermal Characteristics

Parameter(s)	Symbol	Min.	Typ.	Max.	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	—	10.5	—	°C/W
Junction to PCB Thermal Resistance	$\theta_{J\text{-}PCB}$	—	1.4	—	°C/W
Storage Temperature	T_A	−55	—	150	°C
Junction Temperature	T_J	−40	—	150	°C

Notes:

1. θ_{JA} JEDEC JESD 51-2A
2. $\theta_{J\text{-}PCB}$ JEDEC JESD 51-8

4. Typical Performance Curves

The graphs and tables provided in this section are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside the specified power supply range) and therefore outside the warranted range.

Important: Unless otherwise stated, test conditions are $PV_{IN} = V_{IN} = 12V$, $V_{OUT} = 0.6V$, $I_{OUT} = 0A$, PS Resistor = 0Ω, and $C_{OUT} = 10 \times 47\ \mu F$.

Figure 4-1. VOUT vs. Temperature (0.6V)

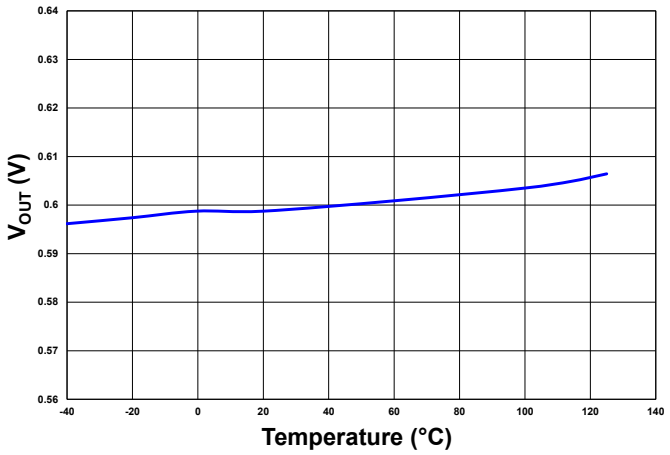


Figure 4-2. VOUT vs. Temperature (0.7V)

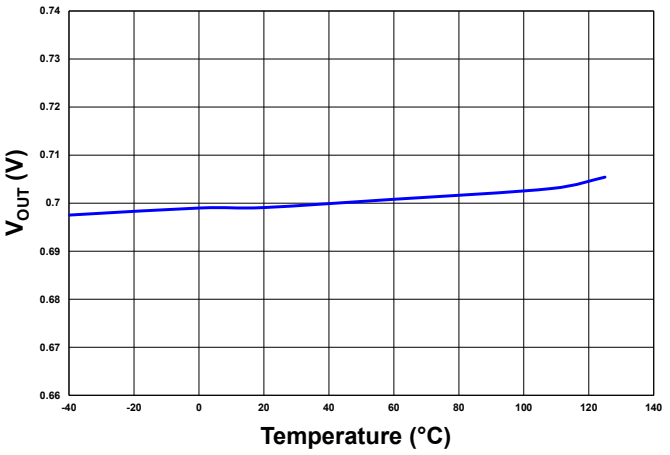


Figure 4-3. VOUT vs. Temperature (0.8V)

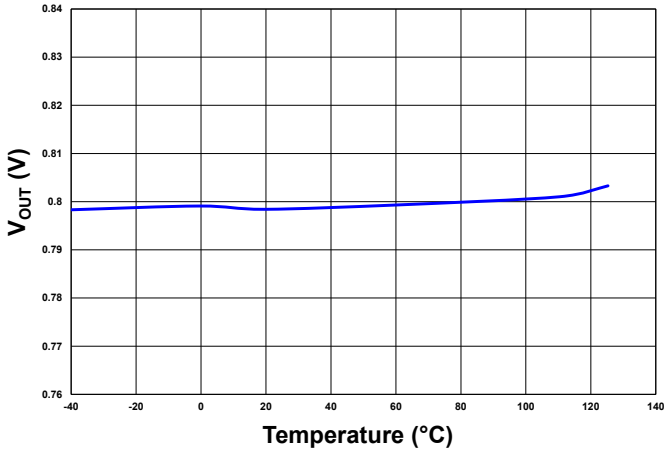


Figure 4-4. VOUT vs. Temperature (0.9V)

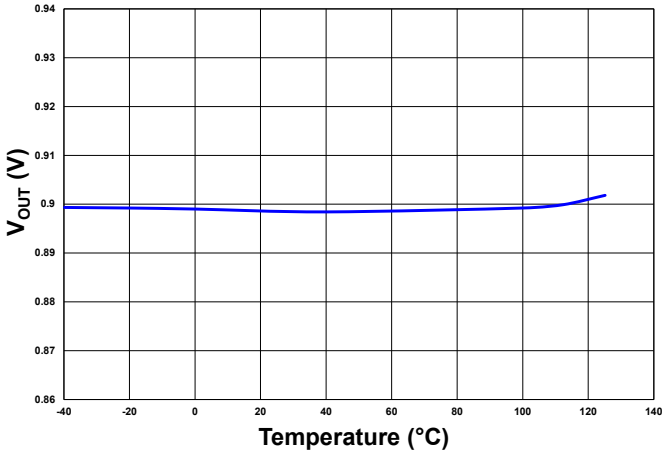


Figure 4-5. VOUT vs. Temperature (1.0V)

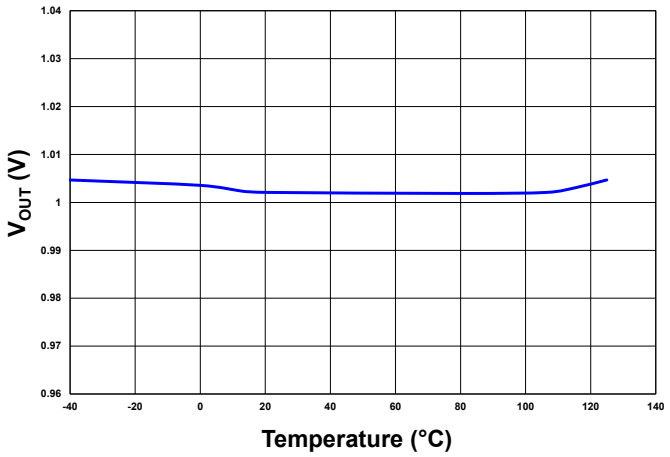


Figure 4-6. VOUT vs. Temperature (1.2V)

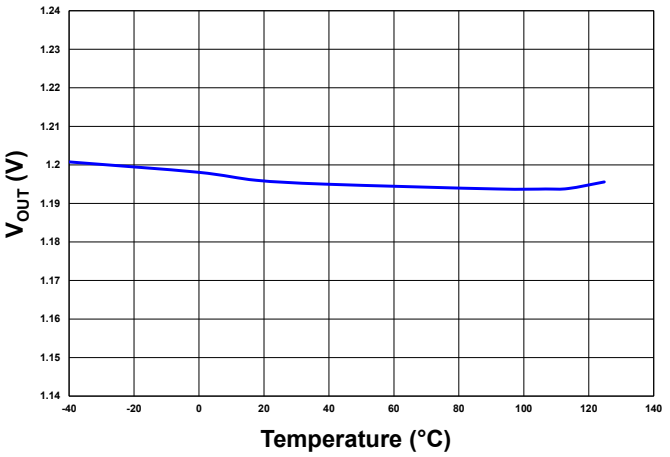


Figure 4-7. VOUT vs. Temperature (1.5V)

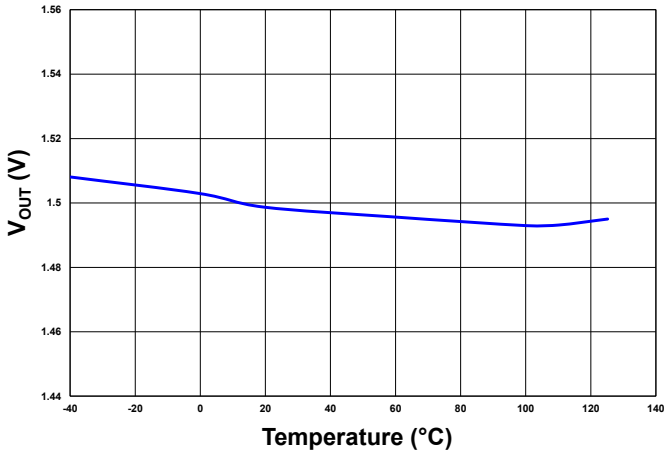


Figure 4-8. VOUT vs. Temperature (1.8V)

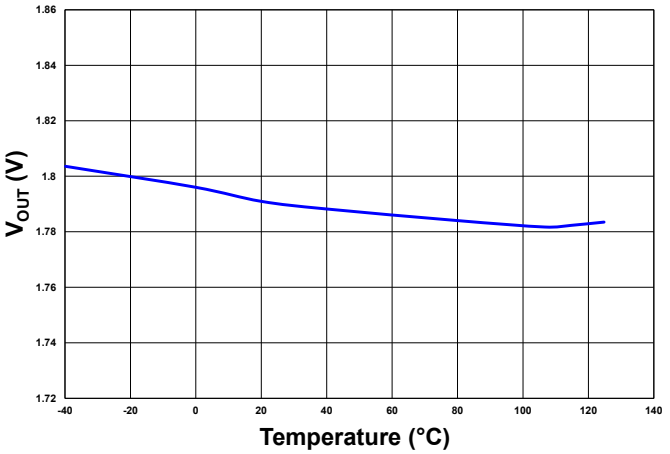


Figure 4-9. EN Start Threshold vs. Temperature

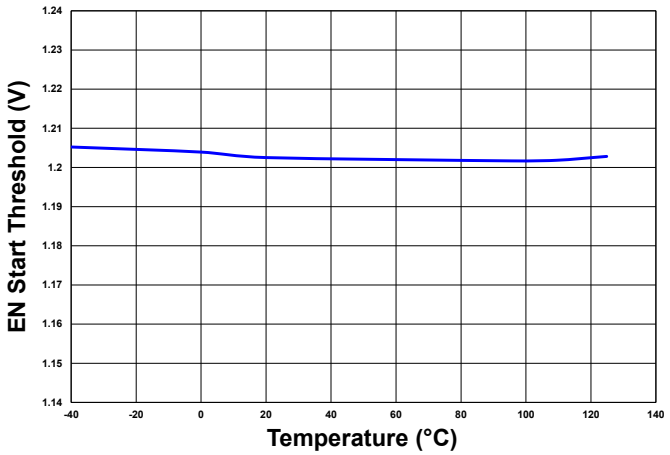


Figure 4-10. EN Stop Threshold vs. Temperature

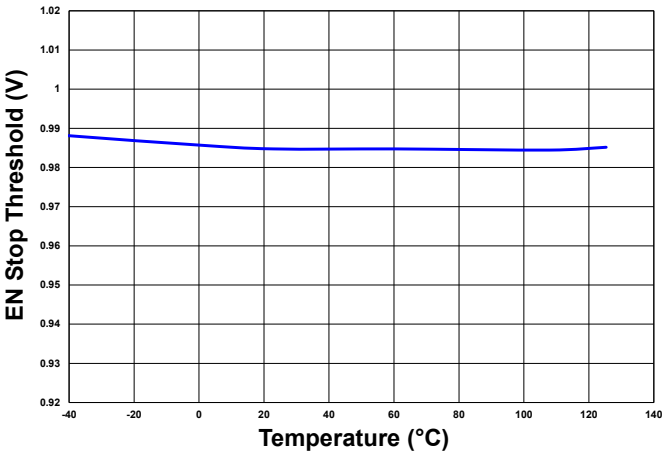


Figure 4-11. VCC Start Threshold vs. Temperature

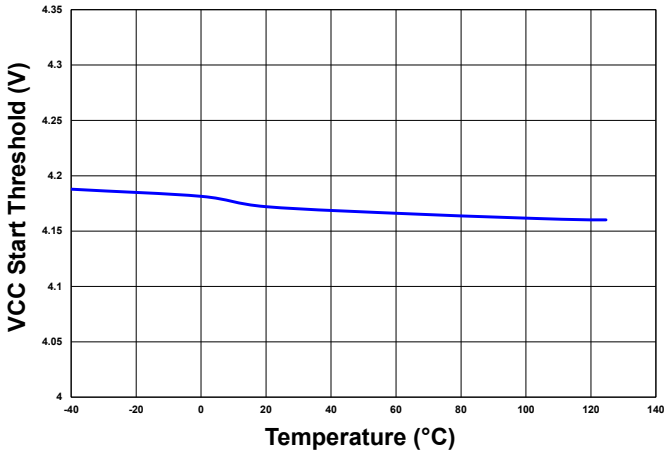


Figure 4-12. VCC Stop Threshold vs. Temperature

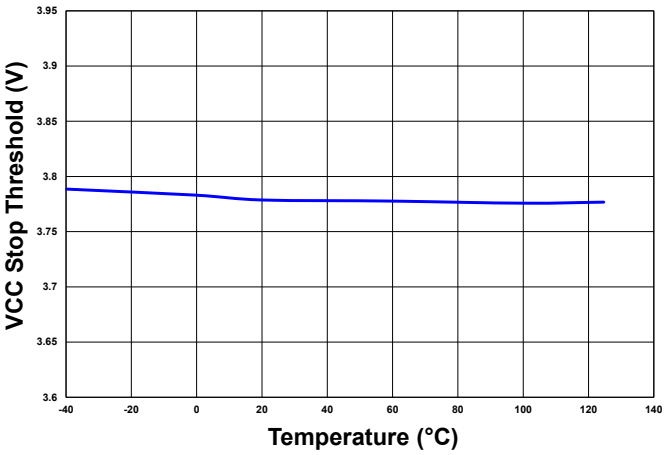


Figure 4-13. t_{ON} vs. Temperature (V_{OUT} = 0.6V, I_{OUT} = 0)

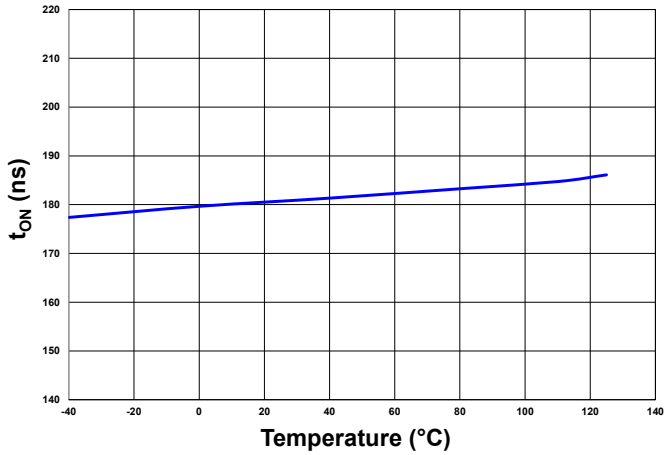


Figure 4-14. t_{OFF} vs. Temperature (PV_{IN} = 6V, V_{IN} = V_{CC} = PV_{CC} = 4.5V)

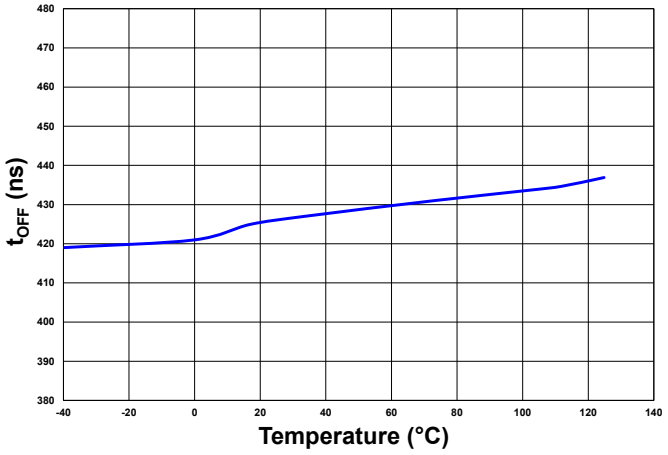


Figure 4-15. Soft Start Time vs. Temperature

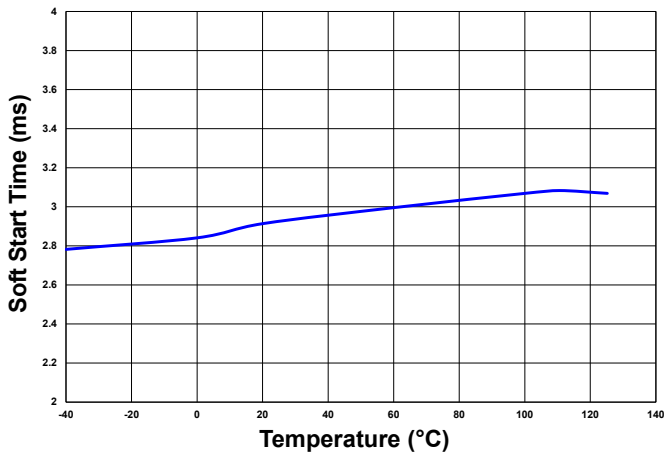


Figure 4-16. VIN Dynamic Input Current vs. Temperature

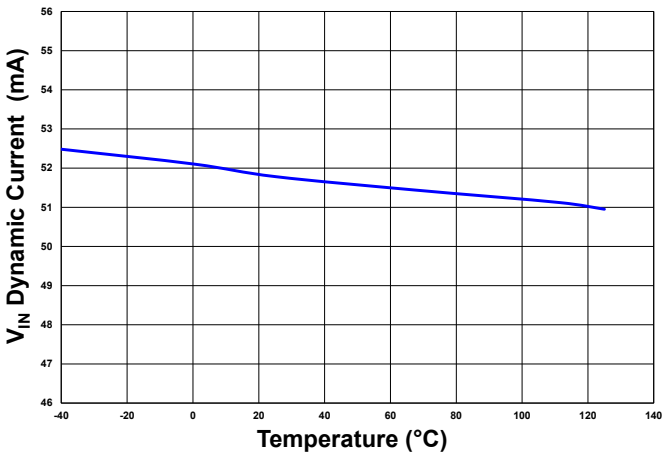


Figure 4-17. Overcurrent Threshold vs. Temperature

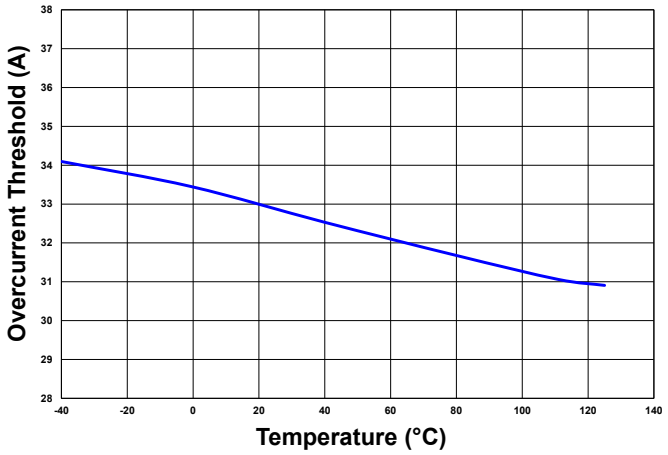


Figure 4-18. Switching Frequency vs. Temperature

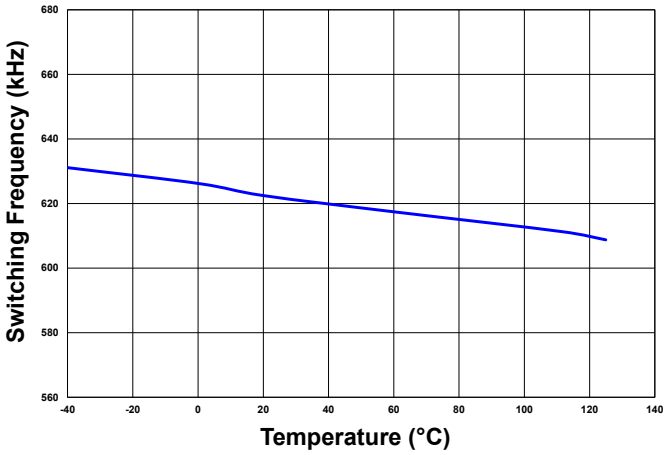


Figure 4-19. Nominal Switching Waveforms (PV_{IN} = 12V, V_{OUT} = 0.6V, I_{OUT} = 0A)

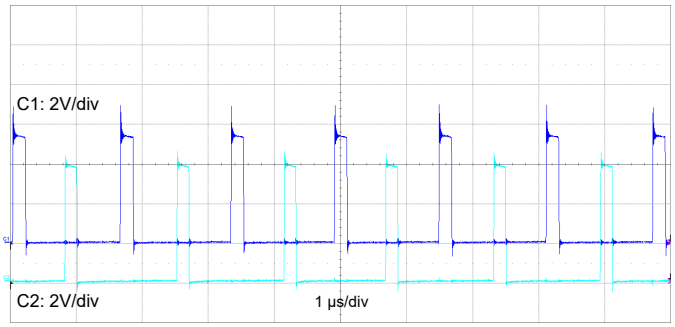


Figure 4-20. Nominal Switching Waveforms (PV_{IN} = 12V, V_{OUT} = 0.6V, I_{OUT} = 25A)

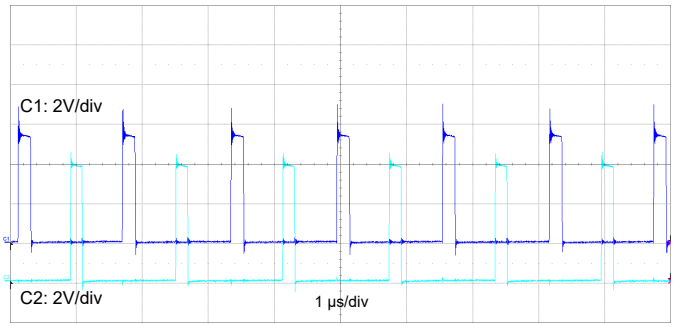


Figure 4-21. Output Ripple (PV_{IN} = 12V, V_{OUT} = 0.6V, I_{OUT} = 0A)

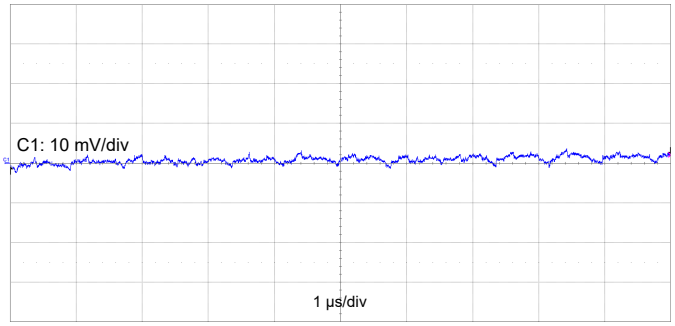


Figure 4-22. Output Ripple (PV_{IN} = 12V, V_{OUT} = 0.6V, I_{OUT} = 25A)

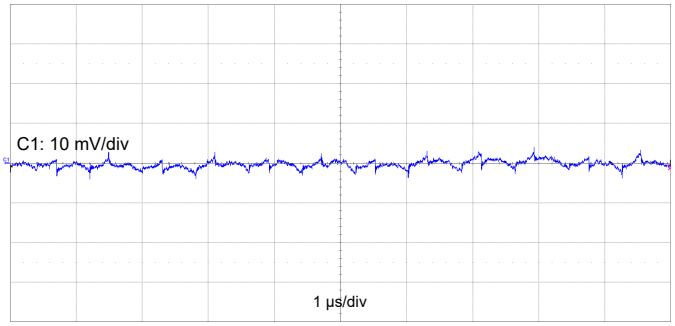


Figure 4-23. Transient (I_{OUT} = 3A to 20A, PV_{IN} = 12V, V_{OUT} = 600 mV)

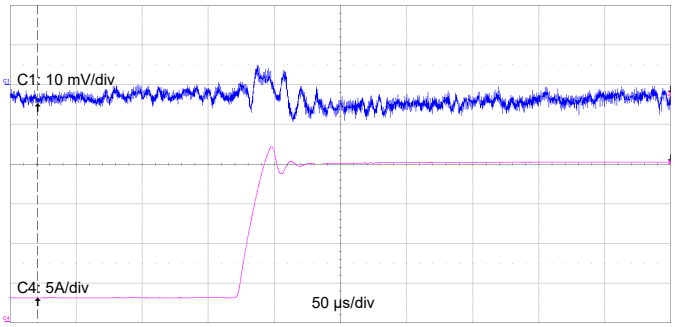


Figure 4-24. Transient (I_{OUT} = 20A to 3A, PV_{IN} = 12V, V_{OUT} = 600 mV)

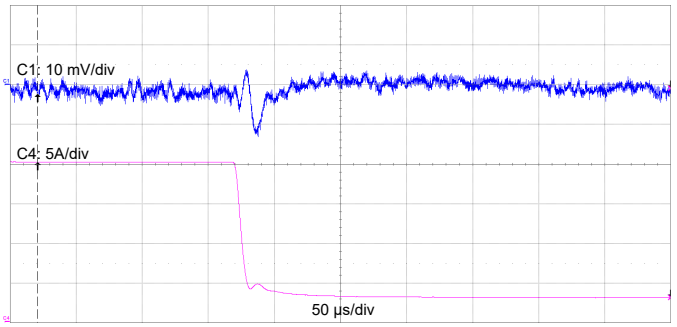


Figure 4-25. Transient (I_{OUT} = 3A to 20A, PV_{IN} = 12V, V_{OUT} = 1V)

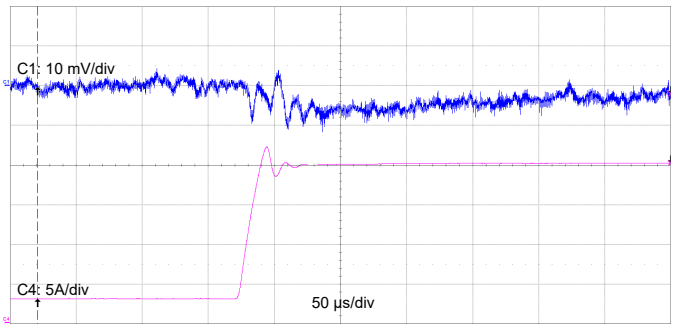


Figure 4-26. Transient (I_{OUT} = 20A to 3A, PV_{IN} = 12V, V_{OUT} = 1V)

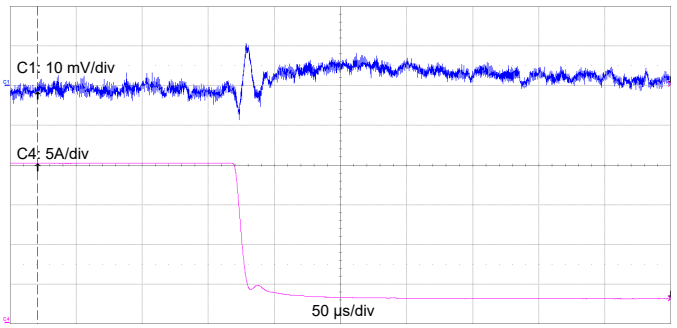


Figure 4-27. Startup (PVIN = 12V, VOUT = 0.6V, IOUT = 0A)

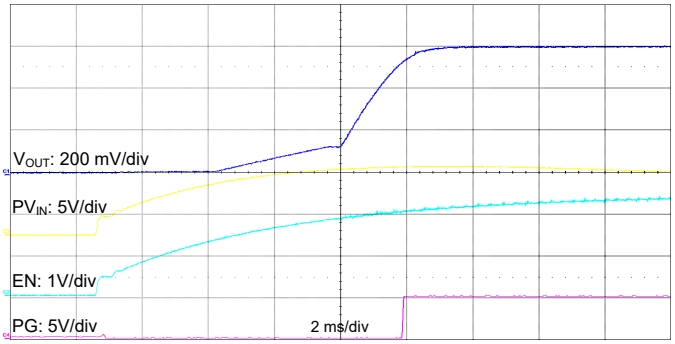


Figure 4-28. Startup (PVIN = 12V, VOUT = 0.6V, IOUT = 16A)

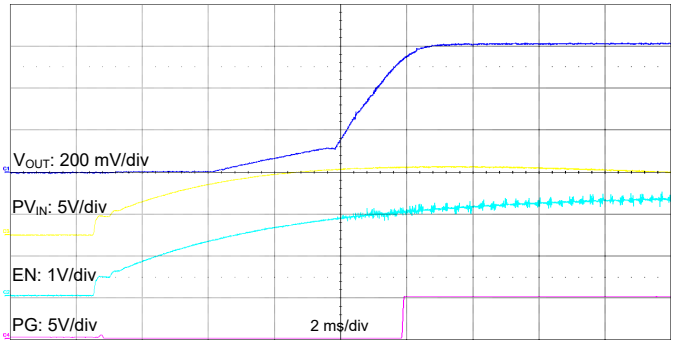


Figure 4-29. Startup (VOUT = 12V to 1V, IOUT = 0A)

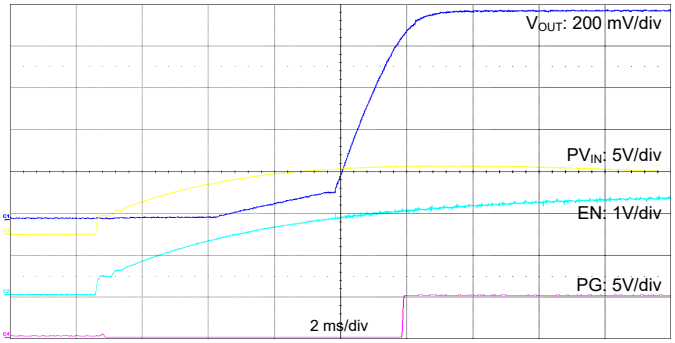


Figure 4-30. Startup (VOUT = 12V to 1V, IOUT = 16A)

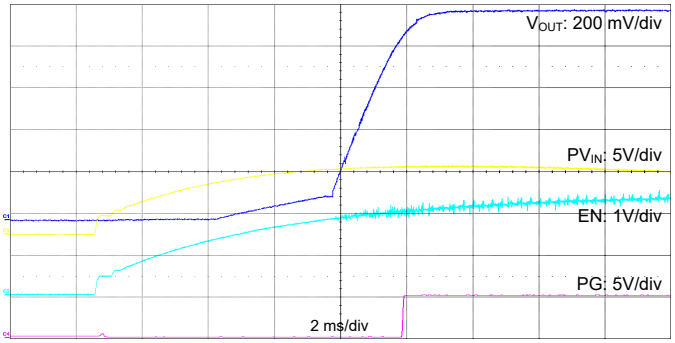


Figure 4-31. Shutdown via EN (VOUT = 12 V to 600 mV, IOUT = 0A)

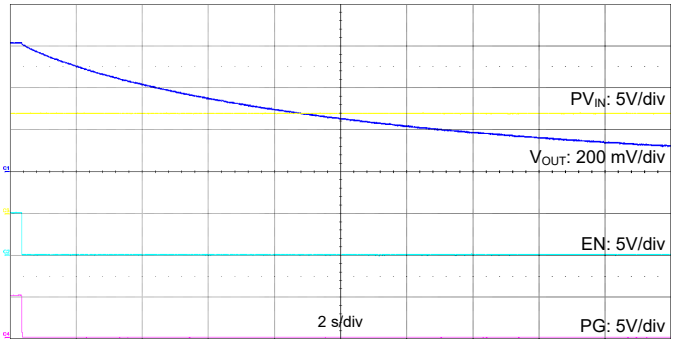


Figure 4-32. Efficiency vs. Load

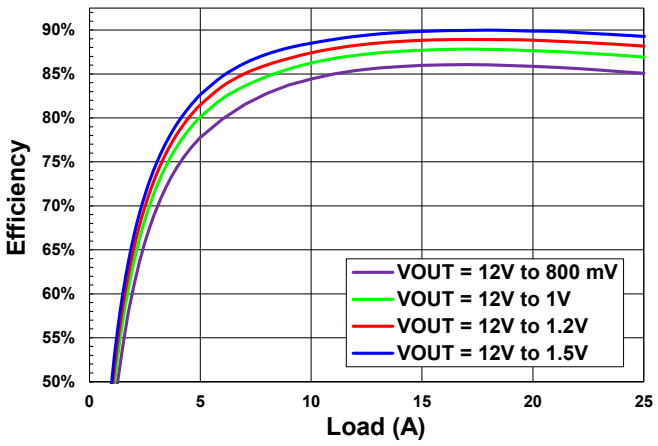


Figure 4-33. Power Loss vs. Load

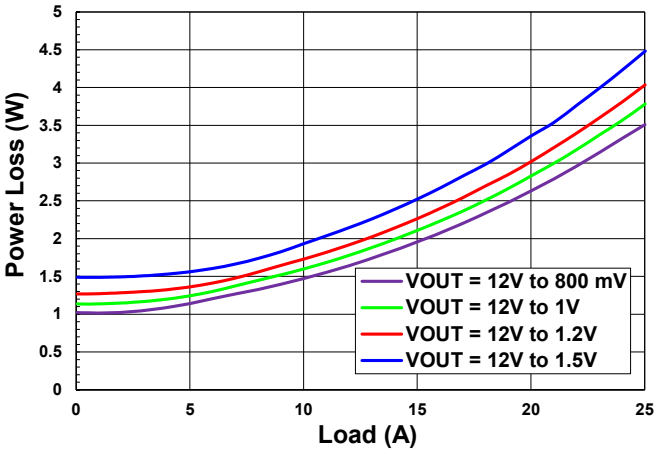


Figure 4-34. Load Regulation vs. Load (VOUT = 12V to 800 mV)

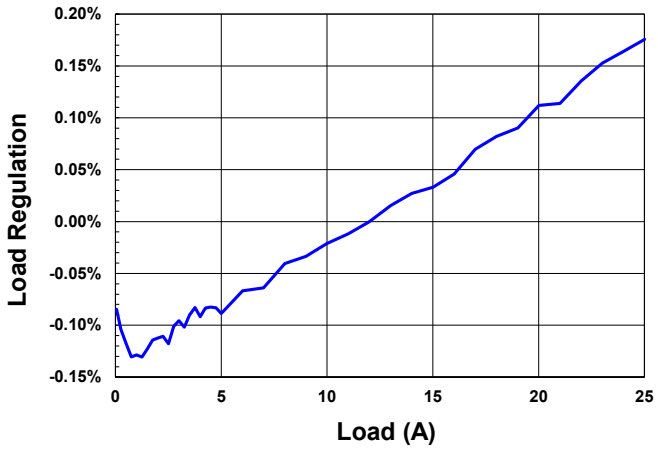


Figure 4-35. Load Regulation vs. Load (VOUT = 12V to 1V)

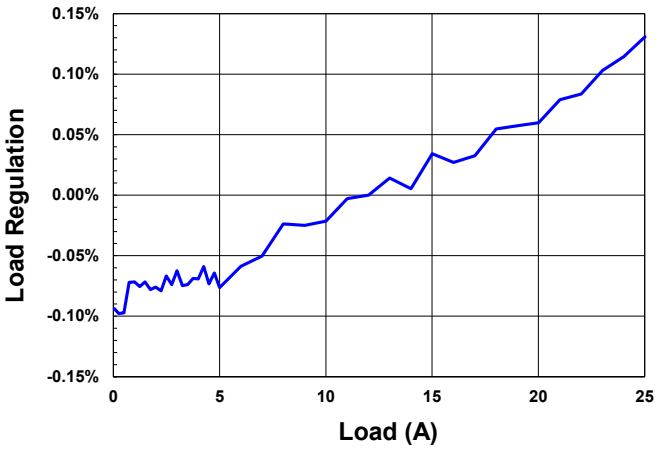


Figure 4-36. Load Regulation vs. Load (VOUT = 12V to 1.2V)

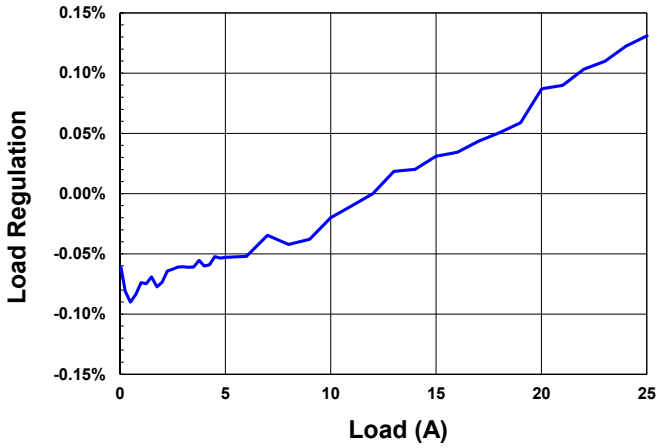
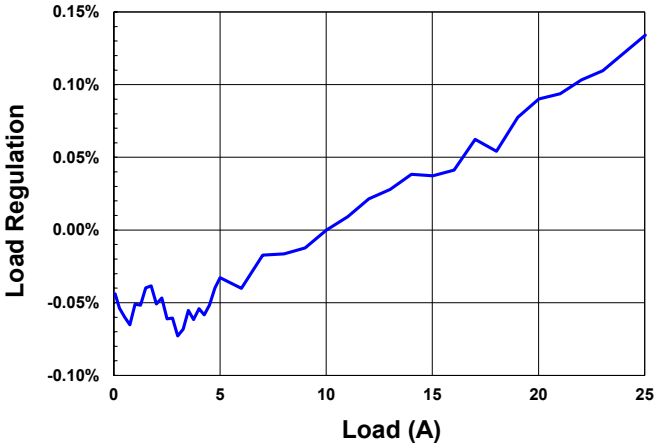


Figure 4-37. Load Regulation vs. Load (VOUT = 12V to 1.5V)



5. Application Information

5.1. Design Example

For this example, the specifications are:

- $PV_{IN} = V_{IN} = 12V$
- $V_{OUT} = 0.8V$
- $I_{OUT} = 25A$
- $f_{SW} = 625$ kHz
- Ripple Voltage = ±1% × V_{OUT}
- $\Delta V_{OUT(MAX)}$ = ±3% × V_{OUT} (for 6A load transient @ 4 A/µs)

5.2. Input Capacitor

The input capacitor chosen for this design must:

- Accommodate the peak and RMS input currents required by the MCPF1525M06
- Possess low equivalent series resistance (ESR) and inductance (ESL) to minimize input voltage disturbances

MLCCs (multi-layer ceramic capacitors) are ideal for this purpose. Typically, in an 0805 case size, they can handle 2A RMS current with less than a 5°C temperature rise. For the MCPF1525M06 converter topology operating at duty cycle D and output current (I_{OUT}), the RMS value of the input current is:

$$I_{RMS} = 0.5 \times I_{OUT} \times \sqrt{D \times (1 - D)}$$

In this application, I_{OUT} is 25A and D is 2 × VOUT/VIN (aggregate duty for a 2-phase converter) or 0.133. Thus, the input capacitor I_{RMS} is 4.25A, so we can choose at least three such capacitors. For this design, four 22 µF, 25V ceramic capacitors are used as the input capacitors (C2012JB1V226M125AC from TDK). If the MCPF1525M06 is not positioned near the 12V power supply, an additional bulk capacitor (68–330 µF) may be used alongside the ceramic capacitors.

For VIN, which serves as the input to the LDO, it is recommended to place a 1 µF capacitor very close to the pin. The VIN pin should be connected to PVIN via a 2.7Ω resistor to help filter noise on PVIN.

5.3. Output Voltage and Output Capacitor

The MCPF1525M06 is factory-calibrated to deliver a 0.6V output in a closed-loop configuration. When opting for a resistor divider instead of using I²C/PMBus™, as illustrated in this application example, resistor values should be selected based on the guidelines provided in Section 'Soft-Start and Target Output Voltage'. Consequently, RTOP is set to 1 kΩ, RBOTTOM to 3.24 kΩ, and CFF to 2.7 nF.

This design uses the TDK C2012X5R1A476M125AC, a 47 µF MLCC with an 0805 case size and a 10V rating. Considering DC bias and AC ripple derating at 0.8V, its equivalent capacitance is approximately 42 µF. The equivalent series resistance (ESR) is 3 mΩ, and the equivalent series inductance (ESL) is 0.44 nH.

5.4. VCC and PVCC Capacitors

The MCPF1525M06 incorporates on-package capacitors for both VCC and PVCC to ensure efficient high-frequency bypassing. However, for applications utilizing an external VCC supply, it is advisable for system designers to place 2.2 µF/0603/X7R/10V capacitors on the application board as close as possible to the VCC and PVCC pins (see Figure 5-1).

5.5. PS Pin Resistance

This pin selects the operating mode for the device. Since this is a stand-alone device and will be using a voltage divider to set the output voltage, a 0Ω resistor is connected from the PS pin

to AGND. Alternatively, an 11 kΩ resistor could be used here and the RSO pin could be directly connected to the FB pin with no divider. See Table 2-3.

5.6. EN Pin Divider

A voltage divider is placed on the EN pin, which is connected to the PVIN pin. This provides a programmable UVLO circuit for the start of power conversion. The turn-on threshold for this pin is 1.2V typical. If the turn-on threshold is set to 6V and the top side resistor (R_{EN1}) is selected as 49.9 kΩ, the bottom resistor (R_{EN2}) can be calculated as follows:

$$R_{EN2} = R_{EN1} \times \frac{V_{EN\_high}}{V_{PVIN\_on} - V_{EN\_high}}$$

Where:

- R_{EN1} and R_{EN2} are the voltage divider resistors on the EN pin
- V_{EN_high} is the turn on threshold of the EN pin (from the Electrical Characteristics table)
- V_{PVIN_on} is the desired PV_{IN} voltage when the device will start power conversion

Using the values mentioned, we select R_{EN2} to be 12.7 kΩ.

Figure 5-1. Design Example

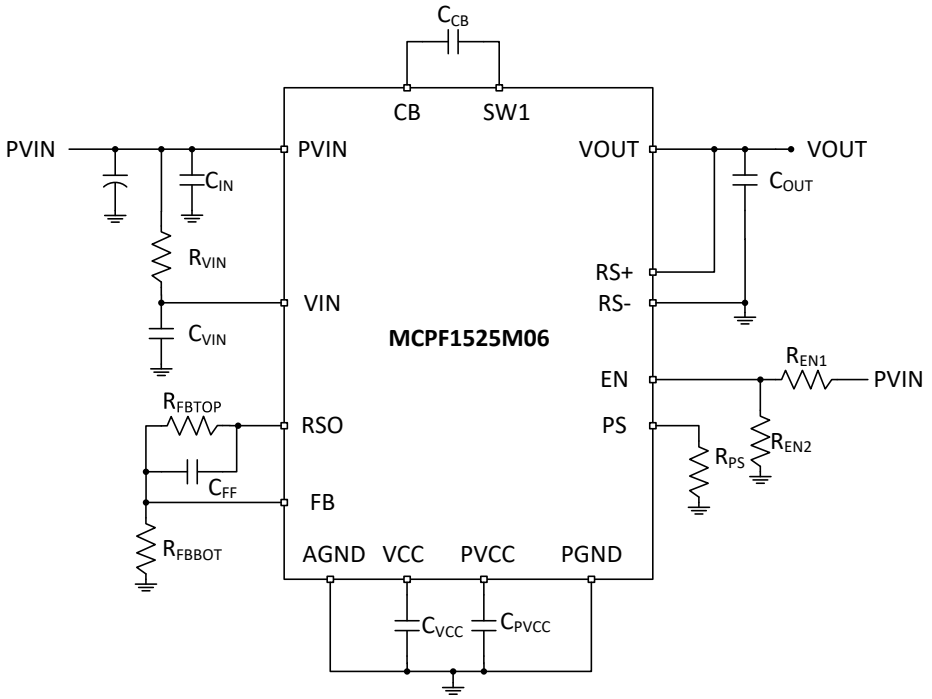


Table 5-1. Final Design:

Component	Value	Component	Value
C_{IN}	4 × 22 µF	R_{VIN}	2.7Ω
C_{VIN}	1 µF	R_{FBTOP}	1 kΩ
C_{FF}	2.7 nF	R_{FBBOT}	3.16 kΩ
C_{VCC}	2.2 µF	R_{PS}	0Ω
C_{PVCC}	2.2 µF	R_{EN1}	49.9 kΩ
C_{OUT}	10 × 47 µF	R_{EN2}	12.7 kΩ
C_{CB}	2 × 4.7 µF		

6. Layout Recommendations

General

The MCPF1525M06 is a highly integrated device that requires minimal external components, making PCB layout straightforward. To ensure optimal performance, follow these general PCB design recommendations:

- Position capacitors and feedback sensing components as close as possible to their corresponding MCPF1525M06's pins.
- Place at least two input capacitors on the top PCB layer, with any additional input capacitors on the bottom layer.
- Install at least two output capacitors on the top layer; any remaining output capacitors can be placed on either the top or bottom layer.
- Mount coupling capacitors between the CB and SW1 pins on the top layer, ensuring robust metal connections.
- Locate coupling capacitors near the VIN, VCC, and PVCC pins, either on the top or bottom layer.
- Use as many decoupling vias as possible on the PVIN, VOUT, PGND, and AGND pins, preferably using vias in pads plated over (VIPPO).
- Place at least two vias adjacent to the PGND and VOUT terminals of each input and output coupling capacitor.
- Route the VOUT remote sensing traces as a differential pair to the load regulation point, ensuring they are positioned away from sources of electrical noise.

Thermal

The MCPF1525M06 has undergone thermal testing and modeling in compliance with JEDEC standards JESD 51-2A and JESD 51-8. Testing was conducted using a 4-layer application PCB equipped with thermal vias beneath the device to enhance cooling.

The MCPF1525M06 has two main heat sources:

- The power MOSFET section of the IC
- The inductor

The IC is effectively coupled to the PCB, which serves as its primary cooling pathway. While the inductor is also connected to the PCB, its main cooling mechanism is through convection. Ultimately, both heat sources dissipate heat through convection. The PCB functions as a heat spreader and, to some extent, a heat sink.

Figure 6-1. Heat Sources in the MCPF1525M06

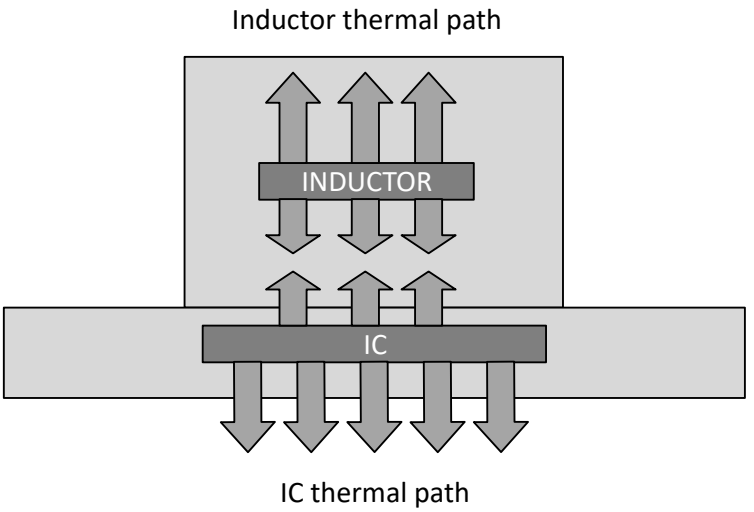


Figure 6-2. Thermal Resistances Components of the MCPF1525M06 Model

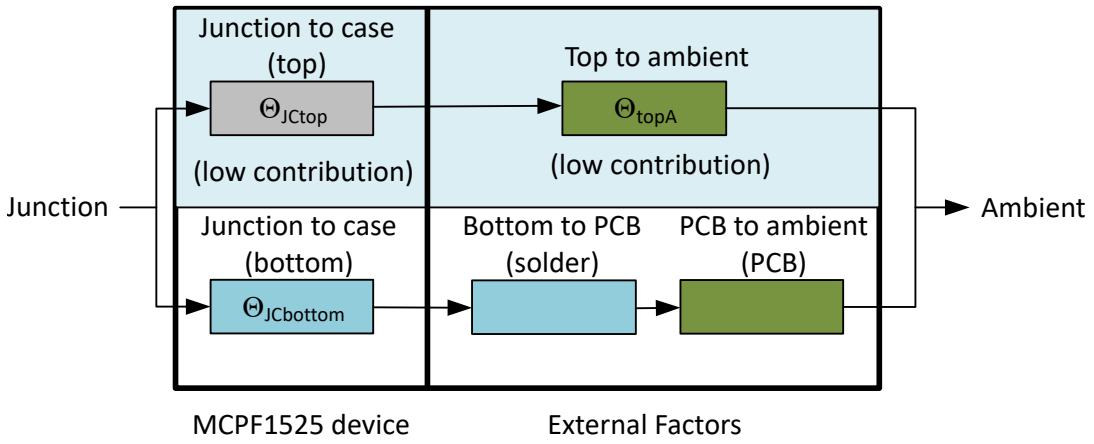


Figure 6-2 illustrates the thermal resistances in the MCPF1525M06, described as follows:

- Θ_{JA} represents the natural convection from the assembled test sample within a confined enclosure of approximately 30 × 30 × 30 cm. The air in this environment is passive, with movement solely due to convection from the device under test.
- $\Theta_{JCbottom}$ indicates the heat flow from the IC to the bottom of the package, where it is well-coupled. The testing method follows JESD 51-8 guidelines, with the test PCB clamped between cold plates at specified distances from the device.
- Θ_{JCtop} theoretically represents the heat flow from the IC to the top of the package. However, this is not applicable for the MCPF1525M06 for two reasons: it is not the primary conduction path of the IC, and the inductor, which generates a similar amount of heat as the IC, is positioned directly over it. Therefore, a meaningful junction-to-case (top) value cannot be determined.

The thermal resistance values are as follows:

- Θ_{JA} = 10.5°C/W
- $\Theta_{JCbottom}$ = 1.4°C/W

While these values provide a comparison of the MCPF1525M06 with similar POL products under identical conditions and specifications, they are not sufficient for predicting overall thermal performance. Precise modeling of the module's interaction with its environment requires Computational Fluid Dynamics (CFD) simulation software to simultaneously calculate the combined effects of conduction and convection heat transfer paths.

Tip: All tests assumed passive or static airflow; applications using forced airflow may achieve better cooling.

Footprint Considerations

The MCPF1525M06 package is compatible with standard surface-mount component techniques. The pads on the bottom of the package are raised slightly above (25 µm) the substrate and are ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold) finished. The package wets well and is suited for lead-free processes. Pads on the board should either be the same size as or slightly larger than the pads on the part substrate.

For best results, it is suggested that the PGND and PVIN pads be connected to inner copper layers using filled vias, micro-vias, or intrusive reflow. This allows the PCB to conduct heat away from the part. The smaller PVIN and PGND pads on the periphery of the part should be connected to the grouped pads beneath the part, as shown in Figure 6-3. These smaller pads are not connected inside the device. Figure 6-4 shows footprint, PCB pad, and solder mask dimensions and outline. Note the solder mask dam between the inner and periphery pads.

Figure 6-3. Pad Grouping and Common Connections

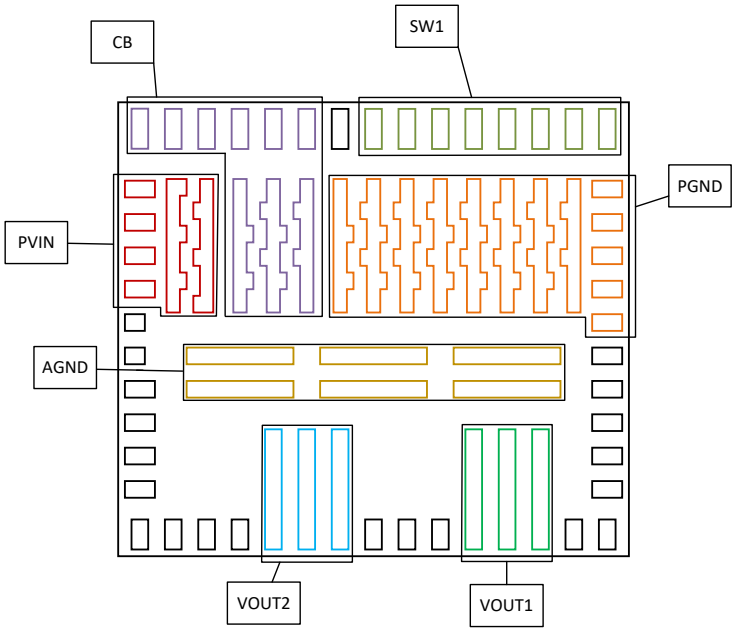
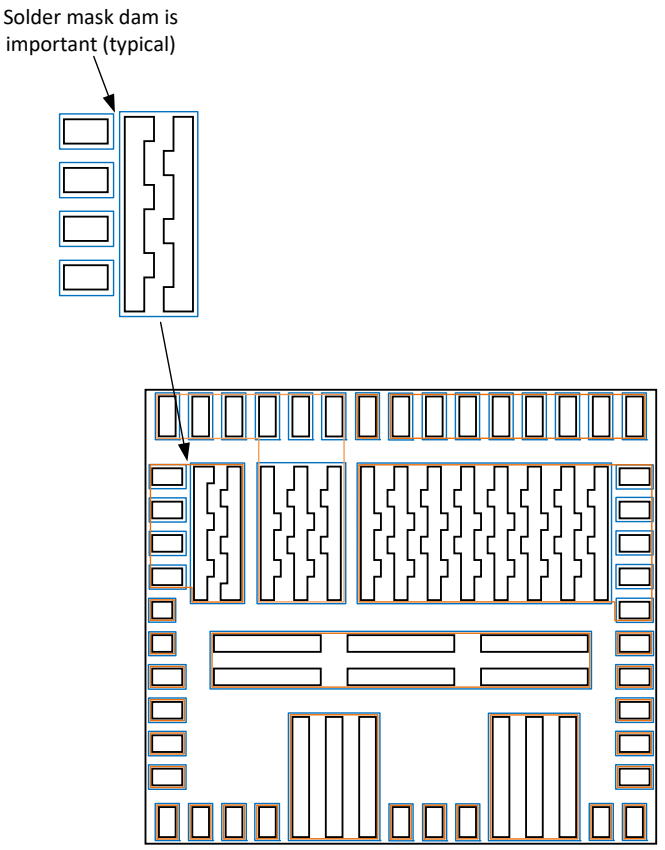


Figure 6-4. Relative Device Footprint, PCB Pad, and Solder Mask Guidelines



7. PMBus Commands

Table 7-1. PMBus Commands List

No.	Name	Adr.	No.	Name	Adr.	No.	Name	Adr.
1	OPERATION	0x01	20	VOUT_OV_WARN_LIMIT	0x42	39	TOFF_FALL	0x65
2	ON_OFF_CONFIG	0x02	21	VOUT_UV_WARN_LIMIT	0x43	40	STATUS_BYTE	0x78
3	CLEAR_FAULTS	0x03	22	VOUT_UV_FAULT_LIMIT	0x44	41	STATUS_WORD	0x79
4	WRITE_PROTECT	0x10	23	VOUT_UV_FAULT_RESPONSE	0x45	42	STATUS_VOUT	0x7A
5	STORE_USER_ALL	0x15	24	IOUT_OC_FAULT_LIMIT	0x46	43	STATUS_IOUT	0x7B
6	RESTORE_USER_ALL	0x16	25	IOUT_OC_FAULT_RESPONSE	0x47	44	STATUS_INPUT	0x7C
7	CAPABILITY	0x19	26	IOUT_OC_WARN_LIMIT	0x4A	45	STATUS_TEMPERATURE	0x7D
8	SMBALERT_MASK	0x1B	27	OT_FAULT_LIMIT	0x4F	46	STATUS_CML	0x7E
9	VOUT_MODE	0x20	28	OT_FAULT_RESPONSE	0x50	47	READ_VIN	0x88
10	VOUT_COMMAND	0x21	29	OT_WARN_LIMIT	0x51	48	READ_VOUT	0x8B
11	VOUT_MAX	0x24	30	VIN_OV_FAULT_LIMIT	0x55	49	READ_IOUT	0x8C
12	VOUT_MARGIN_HIGH	0x25	31	VIN_OV_FAULT_RESPONSE	0x56	50	READ_TEMPERATURE	0x8D
13	VOUT_MARGIN_LOW	0x26	32	VIN_UV_WARN_LIMIT	0x58	51	PMBUS_REVISION	0x98
14	VOUT_TRANSITION_RATE	0x27	33	POWER_GOOD_ON	0x5E	52	MFR_ID	0x99
15	VIN_ON	0x35	34	TON_DELAY	0x60	53	MFR_MODEL	0x9A
16	VIN_OFF	0x36	35	TON_RISE	0x61	54	MFR_REVISION	0x9B
17	IOUT_CAL_OFFSET	0x39	36	TON_MAX_FAULT_LIMIT	0x62	55	IC_DEVICE_ID	0xAD
18	VOUT_OV_FAULT_LIMIT	0x40	37	TON_MAX_FAULT_RESPONSE	0x63	56	IC_DEVICE_REV	0xAE
19	VOUT_OV_FAULT_RESPONSE	0x41	38	TOFF_DELAY	0x64			

OPERATION (0x01)

The OPERATION command is used to turn the device output ON or OFF. It is also used to set the output voltage to the upper or lower MARGIN voltages.

Command	Operation							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

Bit [7]: Controls if PMBus device output is ON or OFF

- 0 : Output is OFF
- 1 : Output is ON

Bit [6]: Controls the power down behavior

- 0 : Output is turned OFF immediately.
- 1 : The device is powered down following the values set in the TOFF_DELAY and TOFF_FALL commands.

Bit [5:4]: Voltage command source

- 00 : The nominal output voltage is set by the PMBus VOUT_COMMAND data
- 01 : The nominal output voltage is set by the PMBus VOUT_MARGIN_LOW data
- 10 : The nominal output voltage is set by the PMBus VOUT_MARGIN_HIGH data
- 11 : AVS Bus (AVS Bus not supported)

Bit [3:2]: Margin fault response

- 00 : Invalid
- 01 : The faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are ignored
- 10 : The faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are acted upon
- 11 : Invalid

Bit [1]: Transition control (AVS Bus not implemented)

Bit [0]: Reserved

ON_OFF_CONFIG (0x02)

Command	ON_OFF_CONFIG							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	1	1	1	1

Bit [7:5]: Reserved

Bit [4]: Sets the default to either operate when power is present or for the ON/OFF to be controlled by serial bus commands

- 0 : Device powers up when the power is present
- 1 : Device does not power up until commanded by the OPERATION command

Bit [3]: Controls how the unit responds to commands received via the serial bus

- 0 : Device ignores the ON/OFF portion of the OPERATION command from serial bus
- 1 : Device requires the ON/OFF portion of the OPERATION command

Bit [2]: Controls how the unit responds to the EN pin

- 0 : Unit ignores the EN pin (ON/OFF controlled only the OPERATION command)
- 1 : Unit requires the EN pin to be asserted to start the unit

Bit [1]: Polarity of the EN pin

- 0 : Active low
- 1 : Active high

Bit [0]: EN pin action

- 0 : Use the programmed turn OFF delay and fall time
- 1 : Turn OFF the output and stop transferring energy to the output as fast as possible

CLEAR_FAULTS (0x03)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device releases its SMBALERT signal output if the device is asserting the SMBALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

WRITE_PROTECT (0x10)

Command	WRITE_PROTECT							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [7]: Control writing to the PMBus device for protection against accidental changes

• 0 : Enable all writes as permitted in bit 5 or bit 6

• 1 : Disable all writes except the WRITE_PROTECT command (bit 5 and bit 6 must be 0)

Bit [6]: Control writing to the PMBus device for protection against accidental changes

• 0 : Enable all writes as permitted in bit 5 or bit 7

• 1 : Disable all writes except for the WRITE_PROTECT, and OPERATION commands (bit 5 and bit 7 must be 0)

Bit [5]: Control writing to the PMBus device for protection against accidental changes

• 0 : Enable all writes as permitted in bit 6 or bit 7

• 1 : Disable all writes except the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND (bit 6 and bit 7 must be 0)

Bit [4:0]: Reserved

STORE_USER_ALL (0x15)

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up. It is permissible to use this command while the device is switching. To use this command:

1. Set all settings to the desired power up configuration.

2. Pull EN low to disable switching.

3. Apply 7.5 ± 0.25V to the VIN pin.

4. Execute the command.

5. Execute a RESTORE_USRE_ALL command.

6. Compare the settings in the part values with the expected settings. If they differ, repeat this procedure. If the settings differ a second time, discard the part.

RESTORE_USER_ALL (0x16)

The RESTORE_USER_ALL command restores all of the storable register settings from EEPROM memory to those registers which are unprotected. This command should not be used while the part is converting power.

CAPABILITY (0x19)

Command	CAPABILITY							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	1	1	0	0	0	0

Bit [7]: Packet Error Checking

• 0 : Packet Error Checking is not supported

Bit [6:5]: Maximum Bus Speed

• 01 : Maximum supported bus speed is 400 kHz

Bit [4]: SMBALERT#

• 1 : The SMBus Alert Response protocol is supported

Bit [3]: Numeric Format

• 0 : Numeric data is in LINEAR11, ULINEAR16, SLINEAR16

Bit [2]: AVSBus Support

• 0 : AVSBus not supported

Bit [1:0]: Reserved

SMBALERT_MASK (0x1B)

The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SMBALERT# signal. The bits in the mask byte align with the bits in the corresponding status register. For example if the STATUS_TEMPERATURE command code were sent with the mask byte 01000000b, then an Overtemperature Warning condition would be blocked from asserting SMBALERT#. This command cannot be used with STATUS_BYTE or STATUS_WORD. Since these commands are the logical or of underlying status registers, use the underlying status commands as the status command code sent to set a mask value. The access mode is a write word transaction for the write and a block write block read transaction for reading. Refer to the SMBus specification for details on this transaction.

VOUT_MODE (0x20)

The data byte for the VOUT_MODE command is one byte that consists of bit [7:5] as Mode and bit[4:0] as Exponent Parameter. The three-bit Mode sets whether the device uses the ULINEAR16, Half-precision IEEE 754 floating point, VID or DIRECT modes for output voltage related commands. The five-bit Parameter provides more information about the selected mode.

Command	VOUT_MODE							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	1	0	0	1	0	1	1	0

Bit [7]: Data type

- 1 : Device supports relative mode

Bit [6:5]: Data type

- 00 : Five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command

Bit [4:0]: Exponent parameter in two's complement

- 10110: value of -10

VOUT_COMMAND (0x21)

The VOUT_COMMAND command sets the output voltage in volts

Command	VOUT_COMMAND															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 format															
Default	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0

Bit [15:0]: Two linear16 data bytes

Note that this part does not use VOUT_SCALE_LOOP. The value provided via the VOUT_COMMAND command is the voltage that the part will regulate the FB pin to. Any voltage divider used on that pin will need to be accounted for by the user when using VOUT_COMMAND.

The default value is 0.5996 (rounded).

VOUT_MAX (0x24)

The VOUT_MAX command sets the maximum output voltage. The purpose is to protect the devices on the output rail supplied by this device from a higher than acceptable output voltage.

Command	VOUT_MAX															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 format															
Default	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit [15:0]: Two linear16 data bytes

The default value is 2.

VOUT_MARGIN_HIGH (0x25)

This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High.”

Command	VOUT_MARGIN_HIGH															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default	0	0	0	0	0	1	0	0	0	1	1	0	0	1	1	0

Bit [15:0]: Two linear16 data bytes

The default value is 1.0996 (rounded).

VOUT_MARGIN_LOW (0x26)

This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low.”

Command	VOUT_MARGIN_LOW															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default	0	0	0	0	0	0	1	1	1	0	0	1	1	0	0	1

Bit [15:0]: Two linear16 data bytes

The default value is 0.8994 (rounded).

VOUT_TRANSITION_RATE (0x27)

VOUT_TRANSITION_RATE command sets the rate in mV/µs at which the output should change voltage.

Command	VOUT_TRANSITION_RATE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Bits [15:11]: A 5 bit, two's complement exponent for the calculation, fixed at –2

Bits [10:0]: An 11 bit, two's complement mantissa for the calculation

Valid range: 0 to 31.75 V/ms

The default value 0.25 V/ms.

VIN_ON (0x35)

The VIN_ON command sets the value of the input voltage, in volts, at which the unit should start power conversion.

Command	VIN_ON															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0

Bits [15:11]: A 5 bit, two's complement exponent for the calculation, fixed at –1

Bits [10:0]: An 11 bit, two's complement mantissa for the calculation

Valid range: 0 to 15.5V

The default value is 3V.

VIN_OFF (0x36)

The VIN_OFF command sets the value of the input voltage, in Volts, at which the unit, once operation has started, should stop power conversion.

Command	VIN_OFF															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0

Bits [15:11]: A 5 bit, two's complement exponent for the calculation, fixed at –1

Bits [10:0]: An 11 bit, two's complement mantissa for the calculation

Valid range: 0 to 15.5V

The default value is 2V.

IOUT_CAL_OFFSET (0x39)

The IOUT_CAL_OFFSET command provides an offset adjustment for the READ_IOUT command. This allows the user to compensate for an offset in the circuit that measures the output current.

Command	IOUT_CAL_OFFSET															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits [15:11]: A 5 bit, two's complement exponent for the calculation, fixed at –4

Bits [10:0]: An 11 bit, two's complement mantissa for the calculation

Valid range: –8A to 8A

The default value is 0A.

VOUT_OV_FAULT_LIMIT (0x40)

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage that causes an output overvoltage fault.

Command	VOUT_OV_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0

Bit [15:0]: A 16 bit, two's complement integer.

The default value is 1.1992 (rounded).

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VOUT_OV_FAULT_RESPONSE (0x41)

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault

Command	VOUT_OV_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption

0x80: Shuts down and does not attempt to restart

0xC0: Shuts down and attempts to restart when the fault condition is no longer present (default)

VOUT_OV_WARN_LIMIT (0x42)

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage that causes an output voltage high warning. This value is typically less than the output overvoltage threshold.

Command	VOUT_OV_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit [15:0]: A 16 bit, two's complement integer

The default value is 4.

VOUT_UV_WARN_LIMIT (0x43)

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage that causes an output voltage low warning. This value is typically greater than the output undervoltage fault threshold.

Command	VOUT_UV_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0

Bit [15:0]: A 16 bit, two's complement integer

The default value is 0.8496 (rounded).

VOUT_UV_FAULT_LIMIT (0x44)

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage that causes an output undervoltage fault. This fault is masked until the unit reaches the programmed output voltage. This fault is also masked when the unit is disabled.

Command	VOUT_UV_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default	0	0	0	0	0		1	1	0	0	1	1	0	0	1	1

Bit [15:0]: A 16 bit, two's complement integer

The default value is 0.7998 (rounded).

VOUT_UV_FAULT_RESPONSE (0x45)

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault.

Command	VOUT_UV_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption (default)

0x80: Shuts down and does not attempt to restart

IOUT_OC_FAULT_LIMIT (0x46)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in Amperes, that causes the overcurrent detector to indicate an overcurrent fault condition.

Command	IOUT_OC_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	1	0	0	0	0	1	0	0	0	0	1	0

Bits [15:11]: A 5 bit, two's complement exponent, fixed at –1

Bits [10:0]: An 11 bit, two's complement mantissa

Valid range: 22 to 37.5A

The default value is 33A.

IOUT_OC_FAULT_RESPONSE (0x47)

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault.

Command	IOUT_OC_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	0	0	0

Valid values:

0xC0: Shuts down and does not attempt to restart

0xF8: Shuts down and attempts to restart continuously (default)

IOUT_OC_WARN_LIMIT (0x4A)

The IOUT_OC_WARN_LIMIT commands sets the output current level in Amperes that cause the part to set the overcurrent warning flag in the STATUS_IOUT register and the corresponding bits in STATUS_BYTE and STATUS_WORD.

Command	IOUT_OC_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0

Bits [15:11]: A 5 bit, two's complement exponent, fixed at –1

Bits [10:0]: An 11 bit, two's complement mantissa

The default value is 28A.

OT_FAULT_LIMIT (0x4F)

The OT_FAULT_LIMIT command sets the temperature, as read by the part for READ_TEMPERATURE, where the over temperature fault will be triggered. This is a different circuit than the analog circuit that sets a firm upper limit on the device temperature of 145°C.

Command	OT_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1

Bits [15:11]: A 5 bit, two's complement exponent, fixed at 0

Bits [10:0]: An 11 bit, two's complement mantissa

Maximum value: 150°C

The default value is 145°C.

OT_FAULT_RESPONSE (0x50)

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an over temperature fault.

Command	OT_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption

0x80: Shuts down and does not attempt to restart

0xC0: Shuts down and attempts to restart when the fault condition is no longer present (default)

Note: The analog over temperature circuit will always cause the part to shut down and restart after cooling.

OT_WARN_LIMIT (0x51)

The OT_WARN_LIMIT command sets the temperature, as read by the part for READ_TEMPERATURE, where the overtemperature issues an overtemperature warning in STATUS_TEMPERATURE.

Command	OT_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits [15:11]: A 5 bit, two's complement exponent, fixed at 0

Bits [10:0]: An 11 bit, two's complement mantissa

Default: 125 °C

Maximum value: 150°C

VIN_OV_FAULT_LIMIT (0x55)

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an Input Overvoltage Fault.

Command	VIN_OV_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits [15:11]: A 5 bit, two's complement exponent for the calculation, fixed at –1

Bits [10:0]: An 11 bit, two's complement mantissa for the calculation

The default value is 18V.

The maximum value is 18V.

VIN_OV_FAULT_RESPONSE (0x56)

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an Input Overvoltage Fault.

Command	VIN_OV_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption (default)

0x80: Shuts down and does not attempt to restart

VIN_UV_WARN_LIMIT (0x58)

The VIN_UV_WARN_LIMIT command sets the value of the input voltage that causes an input voltage low warning. This value is typically greater than the Input Undervoltage Fault threshold, VIN_UV_FAULT_LIMIT.

Command	VIN_UV_WARN_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at –1

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0V to 15.5V

The default value is 3V.

POWER_GOOD_ON (0x5E)

The POWER_GOOD_ON command sets the output voltage at which the POWER_GOOD signal will be asserted, indicating that the output voltage is valid.

Command	POWER_GOOD_ON															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 16 relative format															
Default	0	0	0	0	0	0	1	1	0	1	1	0	0	1	0	1

Bit [15:0]: Two linear16 data bytes

The default value is 0.8486 (rounded).

TON_DELAY (0x60)

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise.

Command	TON_DELAY															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at –1

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.5 ms

The default value is 0 ms.

TON_RISE (0x61)

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. A value of 0 ms instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible.

Command	TON_RISE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at –2

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.75 ms

The default value is 3 ms.

TON_MAX_FAULT_LIMIT (0x62)

The TON_MAX_FAULT_LIMIT command sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. A value of 0 ms means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely.

Command	TON_MAX_FAULT_LIMIT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at –2

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.75 ms

The default value is 0 ms.

TON_MAX_FAULT_RESPONSE (0x63)

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault.

Note: This command must be written twice in succession for changes to take effect.

Command	TON_MAX_FAULT_RESPONSE							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Valid values:

0x00: Continue without interruption (default)

0x80: Shuts down and does not attempt to restart

TOFF_DELAY (0x64)

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output.

Command	TOFF_DELAY															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at –1

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.5 ms

The default value is 0 ms.

TOFF_FALL (0x65)

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-OFF delay time until the voltage is commanded to zero. A value of 0 ms means that the device should ramp the output voltage down as fast as it can.

Command	TOFF_FALL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W, Linear 11 format															
Default	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0

Bit [15:11]: A 5 bit, two's complement exponent, fixed at –2

Bit [10:0]: An 11 bit, two's complement mantissa

Valid range: 0 to 127.75 ms

The default value is 2 ms.

STATUS_BYTE (0x78)

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults.

Command	STATUS_BYTE							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [7]: A fault was declared because the device was busy and unable to respond

Bit [6]: This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled

Bit [5]: An output overvoltage fault has occurred

Bit [4]: An output overcurrent fault has occurred

Bit [3]: An input undervoltage fault has occurred

Bit [2]: A temperature fault or warning has occurred

Bit [1]: A communications, memory or logic fault has occurred

Bit [0]: A fault or warning not listed in bits [7:1] has occurred

STATUS_WORD (0x79)

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

Command	STATUS_WORD (HIGH BYTE)							
Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [15]: An output voltage fault or warning has occurred

Bit [14]: An output current fault or warning has occurred.

Bit [13]: An input voltage fault or warning has occurred

Bit [12]: A manufacturer specific fault or warning has occurred

Bit [11]: The POWER_GOOD signal, if present, is negated

Bit [10]: A fan or airflow fault or warning has occurred (not used)

Bit [9]: A bit in STATUS_OTHER is set (not used)

Bit [8]: A fault type not given in bits [15:1] of the STATUS_WORD

STATUS_VOUT (0x7A)

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults.

Command	STATUS_VOUT							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [7]: OUT_OV_FAULT

Bit [6]: VOUT_OV_WARNING

Bit [5]: VOUT_UV_WARNING

Bit [4]: VOUT_UV_FAULT

Bit [3]: VOUT_MAX_MIN Warning

Bit [2]: TON_MAX_FAULT

Bit [1]: TOFF_MAX_WARNING

Bit [0]: VOUT Tracking Error (not used)

STATUS_IOUT (0x7B)

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.

Command	STATUS_IOUT							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [7]: IOUT_OC_FAULT

Bit [6]: IOUT_OC_LV_FAULT

Bit [5]: IOUT_OC_WARNING

Bit [4]: IOUT_UC_FAULT (not used)

Bit [3]: Current Share Fault (not used)

Bit [2]: In Power Limiting Mode (not used)

Bit [1]: POUT_OP_FAULT (not used)

Bit [0]: POUT_OP_WARNING (not used)

STATUS_INPUT (0x7C)

The STATUS_INPUT command returns one byte of information relating to the status of the input related faults of the converter.

Command	STATUS_INPUT							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [7]: VIN_OV_FAULT

Bit [6]: VIN_OV_WARNING

Bit [5]: VIN_UV_WARNING

Bit [4]: VIN_UV_FAULT

Bit [3]: Unit OFF For Insufficient Input Voltage

Bit [2]: IIN_OC_FAULT (not used)

Bit [1]: IIN_OC_WARNING (not used)

Bit [0]: PIN_OP_WARNING (not used)

STATUS_TEMPERATURE (0x7D)

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the external temperature related faults.

Command	STATUS_TEMPERATURE							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [7]: OT_FAULT

Bit [6]: OT_WARNING

Bit [5]: UT_WARNING (not used)

Bit [4]: UT_FAULT (not used)

Bit [3:0]: Reserved

STATUS_CML (0x7E)

The STATUS_CML command returns one byte of information relating to the status of the communication-related faults of the converter.

Command	STATUS_CML							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [7]: Invalid or unsupported command received

Bit [6]: Invalid or unsupported data received

Bit [5]: Packet error check failed (not used)

Bit [4]: Memory fault detected

Bit [3]: Processor fault detected

Bit [2]: Reserved

Bit [1]: A communication fault other than the ones listed in this table has occurred

Bit [0]: Other memory or logic fault has occurred

READ_VIN (0x88)

The READ_VIN command returns two bytes of data in the linear data format that represent the input voltage of the converter.

Command	READ_VIN															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R, Linear 11 format															
Default	1	1	1	0	0	—	—	—	—	—	—	—	—	—	—	—

Bits [15:11]: A two's complement exponent, –4

Bits [10:0]: An 11 bit two's complement mantissa

READ_VOUT (0x8B)

The READ_VOUT command returns two bytes of data in the linear 16 data format that represent the output voltage of the converter.

Command	READ_VOUT															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R, Linear 16 format															
Default	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bits [15:0]: A two's complement linear 16 format word

READ_IOUT (0x8C)

The READ_IOUT commands returns two bytes of data in the linear 11 data format that represents the output current of the converter.

Command	READ_IOUT										
Bit	15	14	13	12	11	10	9	8	7	6	5
Access	R, Linear 11 format										
Default	1	1	1	0	0	—	—	—	—	—	—

Bits [15:11]: A 5-bit, two's complement exponent, fixed at –4

Bits [10:0]: An 11-bit, two's complement mantissa

READ_TEMPERATURE (0x8D)

The READ_TEMPERATURE command returns the external temperature in degrees Celsius.

Command	READ_TEMPERATURE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R, Linear 11 format															
Default	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—

Bits [15:11]: A two's complement exponent, 0

Bits [10:0]: An 11 bit two's complement mantissa

PMBUS_REVISION (0x98)

PMBUS_REVISION command stores or reads the revision of the PMBus to which the device is compliant.

Command	PMBUS_REVISION							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	1	1	0	0	1	1

Bit [7:4]: Indicate the revision of PMBus specification Part I to which the device is compliant

Value: 0011, PMBus version 1.3

Bit [3:0]: Indicate the revision of PMBus specification Part II to which the device is compliant

Value: 0011, PMBus version 1.3

MFR_ID (0x99)

The MFR_ID command is used to either set or read the manufacturer's ID (name, abbreviation or symbol that identifies the unit's manufacturer). The actual data for this command is 3 bytes. The high order byte here is the byte count in the SMBus block read and block write transactions.

Command	MFR_ID, HIGH TWO BYTES															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	Block R/W															
Default	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	0

Command	MFR_ID, LOW TWO BYTES															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R/W															
Default	0	1	0	0	0	1	0	0	0	1	0	0	1	0	1	1

MFR_MODEL (0x9A)

The MFR_MODEL command is used to either set or read the manufacturer's model number. The actual data for this command is 1 byte. The high order byte here is the byte count in the SMBus block read and block write transactions.

Command	MFR_MODEL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R/W															
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

MFR_REVISION (0x9B)

The MFR_REVISION command is used to either set or read the manufacturer's revision number. The actual data for this command is 1 byte. The high order byte here is the byte count in the SMBus block read and block write transactions.

Command	MFR_REVISION															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R/W															
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

IC_DEVICE_ID (0xAD)

Th IC_DEVICE_ID command is a read-only block-read command that returns 2 bytes with the unique device-code identifier for the device. The actual data for this command is 1 byte. The high order byte here is the byte count in the SMBus block read and block write transactions.

Command	IC_DEV_ID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R															
Default	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1

IC_DEVICE_REV (0xAE)

The IC_DEVICE_REV command is used to read the revision of the IC. The actual data for this command is 1 byte. The high order byte here is the byte count in the SMBus block read and block write transactions.

Command	IC_DEV_REV															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	Block R															
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

8. Register List

Table 8-1. Register List

No.	Name	Adr.	No.	Name	Adr.	No.	Name	Adr.
1	I2C_BASE	0x40	44	OT_FAULT_LIMIT _UPPER	0x6E	87	BOOT_VOLTAGE_1_LOWER	0x9D
2	PMBUS_BASE	0x41	45	OT_FAULT_RESPONSE	0x6F	88	BOOT_VOLTAGE_1_UPPER	0x9E
3	OPERATION	0x42	46	OT_WARN_LIMIT_LOWER	0x70	89	BOOT_VOLTAGE_2_LOWER	0x9F
4	ON_OFF_CONFIG	0x43	47	OT_WARN_LIMIT _UPPER	0x71	90	BOOT_VOLTAGE_2_UPPER	0xA0
5	WRITE_PROTECT	0x44	48	VIN_OV_FAULT_LIMIT_LOWER	0x72	91	BOOT_VOLTAGE_3_LOWER	0xA1
6	MASK_BYTE_VOUT	0x45	49	VIN_OV_FAULT_LIMIT_UPPER	0x73	92	BOOT_VOLTAGE_3_UPPER	0xA2
7	MASK_BYTE_IOUT	0x46	50	VIN_OV_FAULT_RESPONSE	0x74	93	BOOT_VOLTAGE_4_LOWER	0xA3
8	MASK_BYTE_INPUT	0x47	51	VIN_UV_WARN_LIMIT_LOWER	0x75	94	BOOT_VOLTAGE_4_UPPER	0xA4
9	MASK_BYTE_TEMP	0x48	52	VIN_UV_WARN_LIMIT_UPPER	0x76	95	BOOT_VOLTAGE_5_LOWER	0xA5
10	MASK_BYTE_CML	0x49	53	POWER_GOOD_ON_LOWER	0x77	96	BOOT_VOLTAGE_5_UPPER	0xA6
11	VOUT_MODE	0x4B	54	POWER_GOOD_ON_UPPER	0x78	97	BOOT_VOLTAGE_6_LOWER	0xA7
12	VOUT_COMMAND_LOWER	0x4C	55	FAULT_BUS_CONFIG_MASK	0x79	98	BOOT_VOLTAGE_6_UPPER	0xA8
13	VOUT_COMMAND_UPPER	0x4D	56	FAULT_BUS_LATCH_SEL	0x7A	99	BOOT_VOLTAGE_7_LOWER	0xA9
14	VOUT_MAX_LOWER	0x4E	57	TON_DELAY_LOWER	0x7B	100	BOOT_VOLTAGE_7_UPPER	0xAA
15	VOUT_MAX_UPPER	0x4F	58	TON_DELAY_UPPER	0x7C	101	BOOT_VOLTAGE_8_LOWER	0xAB
16	VOUT_MARGIN_HIGH_LOWER	0x50	59	TON_RISE_LOWER	0x7D	102	BOOT_VOLTAGE_8_UPPER	0xAC
17	VOUT_MARGIN_HIGH_UPPER	0x51	60	TON_RISE_UPPER	0x7E	103	STATUS_VOUT	0xC0
18	VOUT_MARGIN_LOW_LOWER	0x52	61	TON_MAX_FAULT_LIMIT_LOWER	0x7F	104	STATUS_IOUT	0xC1
19	VOUT_MARGIN_LOW_UPPER	0x53	62	TON_MAX_FAULT_LIMIT_UPPER	0x80	105	STATUS_INPUT	0xC2
20	VOUT_TRANSITION_RATE_LOWER	0x54	63	TON_MAX_FAULT_RESPONSE	0x81	106	STATUS_TEMPERATURE	0xC3
21	VOUT_TRANSITION_RATE _UPPER	0x55	64	TOFF_DELAY_LOWER	0x82	107	STATUS_CML	0xC4
22	VIN_ON_LOWER	0x58	65	TOFF_DELAY_UPPER	0x83	108	STATUS_BYTE	0xC6
23	VIN_ON _UPPER	0x59	66	TOFF_FALL_LOWER	0x84	109	STATUS_WORD_HIGH	0xC7
24	VIN_OFF_LOWER	0x5A	67	TOFF_FALL_UPPER	0x85	110	BURN_OTP	0xC9
25	VIN_OFF _UPPER	0x5B	68	MFR_ID_COUNT	0x86	111	CLEAR_STATUS	0xCC
26	IOUT_CAL_OFFSET_LOWER	0x5C	69	MFR_ID_1	0x87	112	PVIN_REPORT_LOWER	0xD2
27	IOUT_CAL_OFFSET_UPPER	0x5D	70	MFR_ID_2	0x88	113	PVIN_REPORT_UPPER	0xD3
28	VOUT_OV_FAULT_LIMIT_LOWER	0x5E	71	MFR_ID_3	0x89	114	IOUT_REPORT_LOWER	0xD4
29	VOUT _OV_FAULT_LIMIT_UPPER	0x5F	72	MFR_MODEL_COUNT	0x8A	115	IOUT_REPORT_UPPER	0xD5
30	VOUT _OV_FAULT_RESPONSE	0x60	73	MFR_MODEL	0x8B	116	VOUT_REPORT_LOWER	0xD6
31	VOUT _OV_WARN_LIMIT_LOWER	0x61	74	MFR_REVISION_COUNT	0x8C	117	VOUT_REPORT_UPPER	0xD7
32	VOUT _OV_WARN_LIMIT_UPPER	0x62	75	MFR_REVISION	0x8D	118	TEMP_REPORT_LOWER	0xD8
33	VOUT _UV_WARN_LIMIT_LOWER	0x63	76	FAULT_PIN	0x90	119	TEMP_REPORT_UPPER	0xD9
34	VOUT _UV_WARN_LIMIT_UPPER	0x64	77	BUS_VOLTAGE	0x91	120	VCC_REPORT_LOWER	0xDA
35	VOUT _UV_FAULT_LIMIT_LOWER	0x65	78	CB_OV_UV	0x94	121	VCC_REPORT_UPPER	0xDB
36	VOUT _UV_FAULT_LIMIT_UPPER	0x66	79	CURRENT_REPORT_GAIN	0x95	122	NCL_INDICATION	0xF0
37	VOUT _UV_FAULT_RESPONSE	0x67	80	VOUT_REPORT_GAIN	0x96	123	DAC_CODE	0xF1
38	IOUT_OC_FAULT_LIMIT_LOWER	0x68	81	VOUT_REPORT_OFFSET	0x97	124	USER_OTP_POINTER	0xF2
39	IOUT_OC_FAULT_LIMIT_UPPER	x69	82	PVIN_REPORT_GAIN	0x98	125	STATUS	0xF3
40	IOUT_OC_FAULT_RESPONSE	0x6A	83	PVIN_REPORT_OFFSET	0x99	126	IC_REV_BYTE_COUNT	0xF4
41	IOUT_OC_WARN_LIMIT_LOWER	0x6B	84	TEMP_REPORT_GAIN	0x9A	127	IC_REV	0xF5
42	IOUT_OC_WARN_LIMIT_UPPER	0x6C	85	TEMP_REPORT_OFFSET	0x9B	128	IC_DEV_ID_COUNT	0xF6
43	OT_FAULT_LIMIT_LOWER	0x6D	86	NVM_CRC	0x9C	129	IC_DEV_ID	0xF7

I2C_BASE (0x40)

Register	I2C base Address							
Bit	7	6	5	4	3	2	1	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	0	0	1	0	0	0	0

Bit [7]: Not used

Bits [6:0]: Base address for register level I^2C access

Default value: 0x10

PMBUS_BASE (0x41)

Register	PMBus base Address							
Bit	7	6	5	4	3	2	1	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	1	1	1	0	0	0	0

Bit [7]: Not used

Bits [6:0]: Base address for PMBUS access

Default value: 0x70

OPERATION (0x42)

For a description of this register contents, see the OPERATION command in the PMBus Commands section.

ON_OFF_CONFIG (0x43)

For a description of this register content, see the ON_OFF_CONFIG command in the PMBus Commands section.

WRITE_PROTECT (0x44)

For a description of this register contents, see the WRITE_PROTECT command in the PMBus Commands section. Note that the protections in this register only apply to PMBus access. All access is always available via the direct register level I^2C access.

MASK_BYTE_VOUT (0x45)

This register contains the mask byte applied to the STATUS_VOUT register using the SMBALERT_MASK command.

Register	MASK_BYTE_VOUT							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

MASK_BYTE_IOUT (0x46)

This register contains the mask byte applied to the STATUS_IOUT register using the SMBALERT_MASK command.

Register	MASK_BYTE_IOUT							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

MASK_BYTE_INPUT (0x47)

This register contains the mask byte applied to the STATUS_INPUT register using the SMBALERT_MASK command.

Register	MASK_BYTE_INPUT							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

MASK_BYTE_TEMP (0x48)

This register contains the mask byte applied to the STATUS_TEMP register using the SMBALERT_MASK command.

Register	MASK_BYTE_ TEMP							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

MASK_BYTE_CML (0x49)

This register contains the mask byte applied to the STATUS_CML register using the SMBALERT_MASK command.

Register	MASK_BYTE_ CML							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

VOUT_MODE (0x4B)

For a description of this register contents, see the VOUT_MODE command in the PMBus Commands section.

VOUT_COMMAND_LOWER (0x4C)

For a description of this register contents, see the VOUT_COMMAND command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x4D.

VOUT_COMMAND_UPPER (0x4D)

For a description of this register contents, see the VOUT_COMMAND command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x4C.

VOUT_MAX_LOWER (0x4E)

For a description of this register contents, see the VOUT_MAX command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x4F.

VOUT_MAX_UPPER (0x4F)

For a description of this register contents, see the VOUT_MAX command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x4E.

VOUT_MARGIN_HIGH_LOWER (0x50)

For a description of this register contents, see the VOUT_MARGIN_HIGH command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x51.

VOUT_MARGIN_HIGH_UPPER (0x51)
For a description of this register contents, see the VOUT_MARGIN_HIGH command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x50.

VOUT_MARGIN_LOW_LOWER (0x52)
For a description of this register contents, see the VOUT_MARGIN_LOW command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x53.

VOUT_MARGIN_LOW_UPPER (0x53)
For a description of this register contents, see the VOUT_MARGIN_LOW command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x52

VOUT_TRANSITION_RATE_LOWER (0x54)
For a description of this register contents, see the VOUT_TRANSITION_RATE command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x55.

VOUT_TRANSITION_RATE _UPPER (0x55)
For a description of this register contents, see the VOUT_ TRANSITION_RATE command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x54.

VIN_ON_LOWER (0x58)
For a description of this register contents, see the VIN_ON command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x59.

VIN_ON _UPPER (0x59)
For a description of this register contents, see the VIN_ON command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x58.

VIN_OFF_LOWER (0x5A)
For a description of this register contents, see the VIN_OFF command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x5B.

VIN_OFF _UPPER (0x5B)
For a description of this register contents, see the VIN_OFF command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x5A.

IOUT_CAL_OFFSET_LOWER (0x5C)
For a description of this register contents, see the IOUT_CAL_OFFSET command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x5D.

IOUT_CAL_OFFSET_UPPER (0x5D)
For a description of this register contents, see the IOUT_CAL_OFFSET command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x5C.

VOUT_OV_FAULT_LIMIT_LOWER (0x5E)

For a description of this register contents, see the VOUT_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x5F.

VOUT _OV_FAULT_LIMIT_UPPER (0x5F)

For a description of this register contents, see the VOUT_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x5E.

VOUT _OV_FAULT_RESPONSE (0x60)

For a description of this register contents, see the VOUT_OV_FAULT_RESPONSE command in the PMBus Commands section.

VOUT _OV_WARN_LIMIT_LOWER (0x61)

For a description of this register contents, see the VOUT_OV_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x62.

VOUT _OV_WARN_LIMIT_UPPER (0x62)

For a description of this register contents, see the VOUT_ OV_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x61.

VOUT _UV_WARN_LIMIT_LOWER (0x63)

For a description of this register contents, see the VOUT_UV_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x64.

VOUT _UV_WARN_LIMIT_UPPER (0x64)

For a description of this register contents, see the VOUT_ UV_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x63.

VOUT _UV_FAULT_LIMIT_LOWER (0x65)

For a description of this register contents, see the VOUT_UV_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x66.

VOUT _UV_FAULT_LIMIT_UPPER (0x66)

For a description of this register contents, see the VOUT_ UV_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x65.

VOUT _UV_FAULT_RESPONSE (0x67)

For a description of this register contents, see the VOUT_UV_FAULT_RESPONSE command in the PMBus Commands section.

IOUT_OC_FAULT_LIMIT_LOWER (0x68)

For a description of this register contents, see the IOUT_OC_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x69.

IOUT_OC_FAULT_LIMIT_UPPER (0x69)

For a description of this register contents, see the IOUT_OC_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x68.

IOUT_OC_FAULT_RESPONSE (0x6A)

For a description of this register contents, see the IOUT_OC_FAULT_RESPONSE command in the PMBus Commands section.

IOUT_OC_WARN_LIMIT_LOWER (0x6B)

For a description of this register contents, see the IOUT_OC_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x6C.

IOUT_OC_WARN_LIMIT_UPPER (0x6C)

For a description of this register contents, see the IOUT_OC_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x6B.

OT_FAULT_LIMIT_LOWER (0x6D)

For a description of this register contents, see the OT_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x6E.

OT_FAULT_LIMIT _UPPER (0x6E)

For a description of this register contents, see the OT_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x6D.

OT_FAULT_RESPONSE (0x6F)

For a description of this register contents, see the OT_FAULT_RESPONSE command in the PMBus Commands section.

OT_WARN_LIMIT_LOWER (0x70)

For a description of this register contents, see the OT_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x71.

OT_WARN_LIMIT _UPPER (0x71)

For a description of this register contents, see the OT_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x70.

VIN_OV_FAULT_LIMIT_LOWER (0x72)

For a description of this register contents, see the VIN_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x73.

VIN_OV_FAULT_LIMIT_UPPER (0x73)

For a description of this register contents, see the VIN_OV_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x72.

VIN_OV_FAULT_RESPONSE (0x74)

For a description of this register contents, see the VIN_OV_FAULT_RESPONSE command in the PMBus Commands section.

VIN_UV_WARN_LIMIT_LOWER (0x75)

For a description of this register contents, see the VIN_UV_WARN_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x76.

VIN_UV_WARN_LIMIT_UPPER (0x76)

For a description of this register contents, see the VIN_UV_WARN_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x75.

POWER_GOOD_ON_LOWER (0x77)

For a description of this register contents, see the POWER_GOOD_ON command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x78.

POWER_GOOD_ON_UPPER (0x78)

For a description of this register contents, see the POWER_GOOD_ON command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x77.

FAULT_BUS_CONFIG_MASK (0x79)

This register masks various fault conditions from causing the FAULT pin to assert.

Note: This register must be written twice in succession for changes to take effect.

Register	FAULT_CONFIG_MASK							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7]: Temperature, prevent temperature faults from asserting the FAULT pin

Bit[6]: PVIN, prevent PVIN faults from asserting the FAULT pin

Bit[5]: VOUT, prevent VOUT faults from asserting the FAULT pin

Bit[4]: IOUT, prevent IOUT faults from asserting the FAULT pin

Bit[3]: CLOCK, prevent CLOCK faults from asserting the FAULT pin

Bit[2]: OFF (DA_ENABLE), prevent turning off the part from asserting the FAULT pin

Bit[1]: VCC, prevent VCC faults from asserting the FAULT pin

Bit[0]: Loss of lock, prevent loss of lock faults from asserting the FAULT pin

FAULT_BUS_LATCH_SEL (0x7A)

This register selects which faults will latch, requiring and EN cycle or power cycle to reset

Note: This register must be written twice in succession for changes to take effect.

Register	FAULT_BUS_LATCH_SEL							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	0	0

Bit[7]: CB_UV_OV

Bit[6]: OVP

Bit[5]: VOUT_UV

Bit[4]: TON_MAX

Bit[3]: Overcurrent

Bit[2]: Over temperature

Bit[1]: PVIN_OV

Bit[0]: PVIN_UV

TON_DELAY_LOWER (0x7B)

For a description of this register contents, see the TON_DELAY command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x7C.

TON_DELAY_UPPER (0x7C)

For a description of this register contents, see the TON_DELAY command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x7B.

TON_RISE_LOWER (0x7D)

For a description of this register contents, see the TON_RISE command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x7E.

TON_RISE_UPPER (0x7E)

For a description of this register contents, see the TON_RISE command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x7D.

TON_MAX_FAULT_LIMIT_LOWER (0x7F)

For a description of this register contents, see the TON_MAX_FAULT_LIMIT command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x80.

TON_MAX_FAULT_LIMIT_UPPER (0x80)

For a description of this register contents, see the TON_MAX_FAULT_LIMIT command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x7F.

TON_MAX_FAULT_RESPONSE (0x81)

For a description of this register contents, see the TON_MAX_FAULT_RESPONSE command in the PMBus Commands section.

Note: This register must be written twice in succession for changes to take effect.

TOFF_DELAY_LOWER (0x82)

For a description of this register contents, see the TOFF_DELAY command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x83.

TOFF_DELAY_UPPER (0x83)

For a description of this register contents, see the TOFF_DELAY command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x82.

TOFF_FALL_LOWER (0x84)

For a description of this register contents, see the TOFF_FALL command in the PMBus Commands section. This register contains the low byte of the data for that command. This register requires an atomic write with register 0x85.

TOFF_FALL_UPPER (0x85)

For a description of this register contents, see the TOFF_FALL command in the PMBus Commands section. This register contains the high byte of the data for that command. This register requires an atomic write with register 0x84.

MFR_ID_COUNT (0x86)

Register	MFR_ID_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	1

This register does not have a direct PMBus counterpart but is used in the PMBus MFR_ID command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there are only 3 data bytes available for the MFR_ID command data.

MFR_ID_1 (0x87)

This register contains the first byte used in the PMBus MFR_ID command.

MFR_ID_2 (0x88)

This register contains the second byte (if used) in the PMBus MFR_ID command.

MFR_ID_3 (0x89)

This register contains the third byte (if used) in the PMBus MFR_ID command.

MFR_MODEL_COUNT (0x8A)

Register	MFR_MODEL_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus MFR_ID command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the MFR_MODEL command.

MFR_MODEL (0x8B)

This register contains the byte used in the PMBus MFR_MODEL command.

MFR_REVISION_COUNT (0x8C)

Register	MFR_REVISION_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus MFR_REVISION command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the MFR_MODEL command data.

MFR_REVISION (0x8D)

This register contains the byte used in the PMBus MFR_REVISION command.

FAULT_PIN (0x90)

Register	FAULT_PIN							
Bit	7	6	5	4	3	2	1	0
Access	Reserved	Reserved	Reserved	Reserved	Reserved	R/W	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bits[7:3] Reserved

Bit[2]:

0: Act on FAULT pin signal

1: Ignore FAULT pin signal

Bits[1:0] Reserved

BUS_VOLTAGE (0x91)

Register	BUS_VOLTAGE							
Bit	7	6	5	4	3	2	1	0
Access	Reserved	Reserved	Reserved	R/W	R/W	R/W	Reserved	Reserved
Default	1	1	1	0	1	0	0	0

This register sets the bus voltage for the I^2C bus, PLL mode and power good behavior.

Bit [4]:

0: Enable PLL, Mode B

1: Disable PLL, Mode A (default)

Bit [3]:

0: Power Good based on POWER_GOOD_ON command value

1: Power Good based on DAC (default)

Bit [2]:

0: 1.8V to 2.5V I^2C bus voltage (default)

1: 3.3V to 5V I^2C bus voltage

All other bits are reserved.

CB_OV_UV (0x94)

Register	CB_OV_UV							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Reserved	R/W	Reserved	Reserved	Reserved	Reserved
Default	—	—	0	1	0	0	0	1

This register is used to enable the OV and UV functions for the CB capacitor.

Bit[4]: CB_OV_UV_ENABLE

0: CB OV/UV function disabled. Set to 0 for PVIN < 8V.

1: CB OV/UV function enabled. Set to 0 for PVIN > 8V, default.

CURRENT_REPORT_GAIN (0x95)

Register	CURRENT_REPORT_GAIN							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

This register allows setting the gain for the reporting of output current. The resolution is 1/256 with 0 being a gain of 0 and 255 being a gain of 1.

VOUT_REPORT_GAIN (0x96)

Register	VOUT_REPORT_GAIN							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

This register allows setting the gain for the reporting of output voltage. The resolution is 1/256 with 0 being a gain of 0.5 and 255 being a gain of 1.5.

VOUT_REPORT_OFFSET (0x97)

Register	VOUT_REPORT_OFFSET							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register allows setting the offset for the reporting of output voltage. The resolution is 1/1024.

PVIN_REPORT_GAIN (0x98)

Register	PVIN_REPORT_GAIN							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

This register allows setting the gain for the reporting of input voltage. The resolution is 1/256 with 0 being a gain of 0.5 and 255 being a gain of 1.5.

PVIN_REPORT_OFFSET (0x99)

Register	PVIN_REPORT_OFFSET							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register allows setting the offset for the reporting of input voltage. The resolution is 1/16.

TEMP_REPORT_GAIN (0x9A)

Register	TEMP_REPORT_GAIN							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0

This register allows setting the gain for the reporting of device temperature. The resolution is 1/256.

TEMP_REPORT_OFFSET (0x9B)

Register	TEMP_REPORT_OFFSET							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register allows setting the offset for the reporting of Device temperature. The resolution is 1°C.

NVM_CRC (0x9C)

Register	NVM_CRC							
Bit	7	6	5	4	3	2	1	CRC_EN
Access	Unused	Unused	Unused	Unused	Unused	Reserved	Reserved	R/W
Default	—	—	—	—	—	0	0	0

This register enables or disables a CRC function in the non-volatile memory. When enabled, two of the 12 banks of memory are used for each memory write. On a new part, this would leave 5 banks available for writing by the end user when enabled. If not enabled, a new part will have 11 banks available.

Bit [0]: CRC_ENABLE

0: CRC is disabled, default

1: CRC is enabled

BOOT_VOLTAGE_1_LOWER (0x9D)

This register must be atomically written with register BOOT_VOLTAGE_1_UPPER

Register	BOOT_VOLTAGE_1_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	0	1	1

This register along with register 0x9E set the default output voltage when the PS pin resistor is 6.34 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_1_UPPER (0x9E)

This register must be atomically written with register BOOT_VOLTAGE_1_LOWER

Register	BOOT_VOLTAGE_1_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0x9D set the default output voltage when the PS pin resistor is 6.34 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_2_LOWER (0x9F)

This register must be atomically written with register BOOT_VOLTAGE_2_UPPER.

Register	BOOT_VOLTAGE_2_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	1	1	0	0

This register along with register 0xA0 set the default output voltage when the PS pin resistor is 7.15 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_2_UPPER (0xA0)

This register must be atomically written with register BOOT_VOLTAGE_2_LOWER.

Register	BOOT_VOLTAGE_2_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0x set the default output voltage when the PS pin resistor is 7.15 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_3_LOWER (0xA1)

This register must be atomically written with register BOOT_VOLTAGE_3_UPPER.

Register	BOOT_VOLTAGE_3_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	0	1	1

This register along with register 0xA2 set the default output voltage when the PS pin resistor is 7.87 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_3_UPPER (0xA2)

This register must be atomically written with register BOOT_VOLTAGE_3_LOWER.

Register	BOOT_VOLTAGE_3_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0xA1 set the default output voltage when the PS pin resistor is 7.87 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_4_LOWER (0xA3)

This register must be atomically written with register BOOT_VOLTAGE_4_UPPER.

Register	BOOT_VOLTAGE_4_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	0	1	1

This register along with register 0xA4 set the default output voltage when the PS pin resistor is 8.66 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_4_UPPER (0xA4)

This register must be atomically written with register BOOT_VOLTAGE_4_LOWER.

Register	BOOT_VOLTAGE_4_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0xA3 set the default output voltage when the PS pin resistor is 8.66 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_5_LOWER (0xA5)

This register must be atomically written with register BOOT_VOLTAGE_5_UPPER.

Register	BOOT_VOLTAGE_5_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	1	0	0	0	0

This register along with register 0xA6 set the default output voltage when the PS pin resistor is 9.31 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_5_UPPER (0xA6)

This register must be atomically written with register BOOT_VOLTAGE_5_LOWER.

Register	BOOT_VOLTAGE_5_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0xA5 set the default output voltage when the PS pin resistor is 9.31 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_6_LOWER (0xA7)

This register must be atomically written with register BOOT_VOLTAGE_6_UPPER.

Register	BOOT_VOLTAGE_6_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	0	1	1	0

This register along with register 0xA8 set the default output voltage when the PS pin resistor is 10.2 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_6_UPPER (0xA8)

This register must be atomically written with register BOOT_VOLTAGE_6_LOWER.

Register	BOOT_VOLTAGE_6_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0xA7 set the default output voltage when the PS pin resistor is 10.2 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_7_LOWER (0xA9)

This register must be atomically written with register BOOT_VOLTAGE_7_UPPER.

Register	BOOT_VOLTAGE_7_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	1	1	0	1	1

This register along with register 0xAA set the default output voltage when the PS pin resistor is 11 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_7_UPPER (0xAA)

This register must be atomically written with register BOOT_VOLTAGE_7_LOWER.

Register	BOOT_VOLTAGE_7_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0xA9 set the default output voltage when the PS pin resistor is 11 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_8_LOWER (0xAB)

This register must be atomically written with register BOOT_VOLTAGE_8_UPPER.

Register	BOOT_VOLTAGE_8_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	0	0	0

This register along with register 0xAC set the default output voltage when the PS pin resistor is 12.1 kΩ. See the PS pin section for more details.

BOOT_VOLTAGE_8_UPPER (0xAC)

This register must be atomically written with register BOOT_VOLTAGE_8_LOWER.

Register	BOOT_VOLTAGE_8_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	Unused	R/W
Default	0	0	0	0	0	0	0	0

This register along with register 0xAB set the default output voltage when the PS pin resistor is 12.1 kΩ. See the PS pin section for more details.

STATUS_VOUT (0xC0)

For a description of this register contents, see the STATUS_VOUT command in the PMBus Commands section.

STATUS_IOUT (0xC1)

For a description of this register contents, see the STATUS_IOUT command in the PMBus Commands section.

STATUS_INPUT (0xC2)

For a description of this register contents, see the STATUS_INPUT command in the PMBus Commands section.

STATUS_TEMPERATURE (0xC3)

For a description of this register contents, see the STATUS_TEMPERATURE command in the PMBus Commands section.

STATUS_CML (0xC4)

For a description of this register contents, see the STATUS_CML command in the PMBus Commands section.

STATUS_BYTE (0xC6)

For a description of this register contents, see the STATUS_BYTE command in the PMBus Commands section.

STATUS_WORD_HIGH (0xC7)

For a description of this register contents, see the STATUS_WORD command in the PMBus Commands section. This register is the high byte of that command.

BURN_OTP (0xC9)

Register	BURN_OTP							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Unused	R/W	Reserved
Default	0	0	0	0	0	0	0	0

Bits[7:2] – unused

Bit[1] – set to 1 to burn the OTP

Bit[0] – reserved

CLEAR_STATUS (0xCC)

Register	CLEAR_STATUS							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	Reserved	Reserved	R/W
Default	0	0	0	0	0	0	1	0

Bits[7:3] – unused

Bits[2:1] – reserved

Bit[0] – set to 1 to clear the status flags

PVIN_REPORT_LOWER (0xD2)

For a description of this register contents, see the READ_VIN command in the PMBus Commands section. This register contains the low byte of the data for that command.

PVIN_REPORT_UPPER (0xD3)

For a description of this register contents, see the READ_VIN command in the PMBus Commands section. This register contains the high byte of the data for that command.

IOUT_REPORT_LOWER (0xD4)

For a description of this register contents, see the READ_IOUT command in the PMBus Commands section. This register contains the low byte of the data for that command.

IOUT_REPORT_UPPER (0xD5)

For a description of this register contents, see the READ_IOUT command in the PMBus Commands section. This register contains the high byte of the data for that command.

VOUT_REPORT_LOWER (0xD6)

For a description of this register contents, see the READ_VOUT command in the PMBus Commands section. This register contains the low byte of the data for that command.

VOUT_REPORT_UPPER (0xD7)

For a description of this register contents, see the READ_VOUT command in the PMBus Commands section. This register contains the high byte of the data for that command.

TEMP_REPORT_LOWER (0xD8)

For a description of this register contents, see the READ_TEMPERATURE command in the PMBus Commands section. This register contains the low byte of the data for that command.

TEMP_REPORT_UPPER (0xD9)

For a description of this register contents, see the READ_TEMPERATURE command in the PMBus Commands section. This register contains the high byte of the data for that command.

VCC_REPORT_LOWER (0xDA)

Register	VCC_REPORT_LOWER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	—	—	—	—	—	—	—	—

This register contains the low byte of a linear 11 format representation of the VCC voltage of the part.

VCC_REPORT_UPPER (0xDB)

Register	VCC_REPORT_UPPER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	—	—	—	—	—	—	—	—

This register contains the high byte of a linear 11 format representation of the VCC voltage of the part. The exponent for this calculation, with a value of -5, is in bits [7:3].

NCL_INDICATION (0xF0)

Register	NCL_INDICATION							
Bit	7	6	5	4	3	2	1	0
Access	Unused	Unused	Unused	Unused	Unused	R	R	R
Default	—	—	—	—	1	0	0	—

This register shows a negative current limit indication for each of the two phases and the high bit of the actual reference DAC.

Bits[7:3]: Unused

Bit[2]: NCL for phase 1

Bit[1]: NCL for phase 2

Bit[0]: High bit for the reference DAC

DAC_CODE (0xF1)

Register	DAC_CODE							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	—	—	—	—	—	—	—	—

This register shows the lower 8 bits of the reference DAC.

Bits{7:0]: Low 8 bits of the reference DAC

USER_OTP_POINTER (0xF2)

Register	USER_OTP_POINTER							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	Reserved	Reserved	Reserved	Reserved
Default	1	0	1	1	—	—	—	—

Bits[7:4]

0001: 1 write remaining

0010: 2 writes remaining

0011: 3 writes remaining

0100: 4 writes remaining

0101: 5 writes remaining

0110: 6 writes remaining

0111: 7 writes remaining

1000: 8 writes remaining

1001: 9 writes remaining

1010: 10 writes remaining

1011: 11 writes remaining, default for a new part

1100: 12 writes remaining

STATUS (0xF3)

Register	STATUS							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

This register shows the status flags for the part.

Bit [7]: Power Good status

Bit [6]: Overvoltage status

Bit [5]: Overcurrent status

Bit [4]: Temperature status

Bit [3]: Enable pin status

Bit [2]: Not used

Bit [1]: User NVM write status

Bit [0]: Status cleared indicator. This is a mirror of register 0xCC, bit 0.

IC_REV_BYTE_COUNT (0xF4)

Register	IC_REV_BYTE_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus IC_DEVICE_REV command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the IC_DEVICE_REV command.

IC_REV (0xF5)

This register contains the byte used in the PMBus IC_DEVICE_REV command.

Register	IC_REV							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

IC_DEV_ID_COUNT (0xF6)

Register	IC_DEV_ID_COUNT							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

This register does not have a direct PMBus counterpart but is used in the PMBus IC_DEVICE_ID command. This command is a SMBus block read or a SMBus block write command. This register holds the byte count for these SMBus transactions. Note that there is only 1 data byte available for the IC_DEVICE_REV command.

IC_DEV_ID (0xF7)

This register contains the byte used in the PMBus IC_DEVICE_ID command.

Register	IC_DEV_ID							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	1	0	0	1

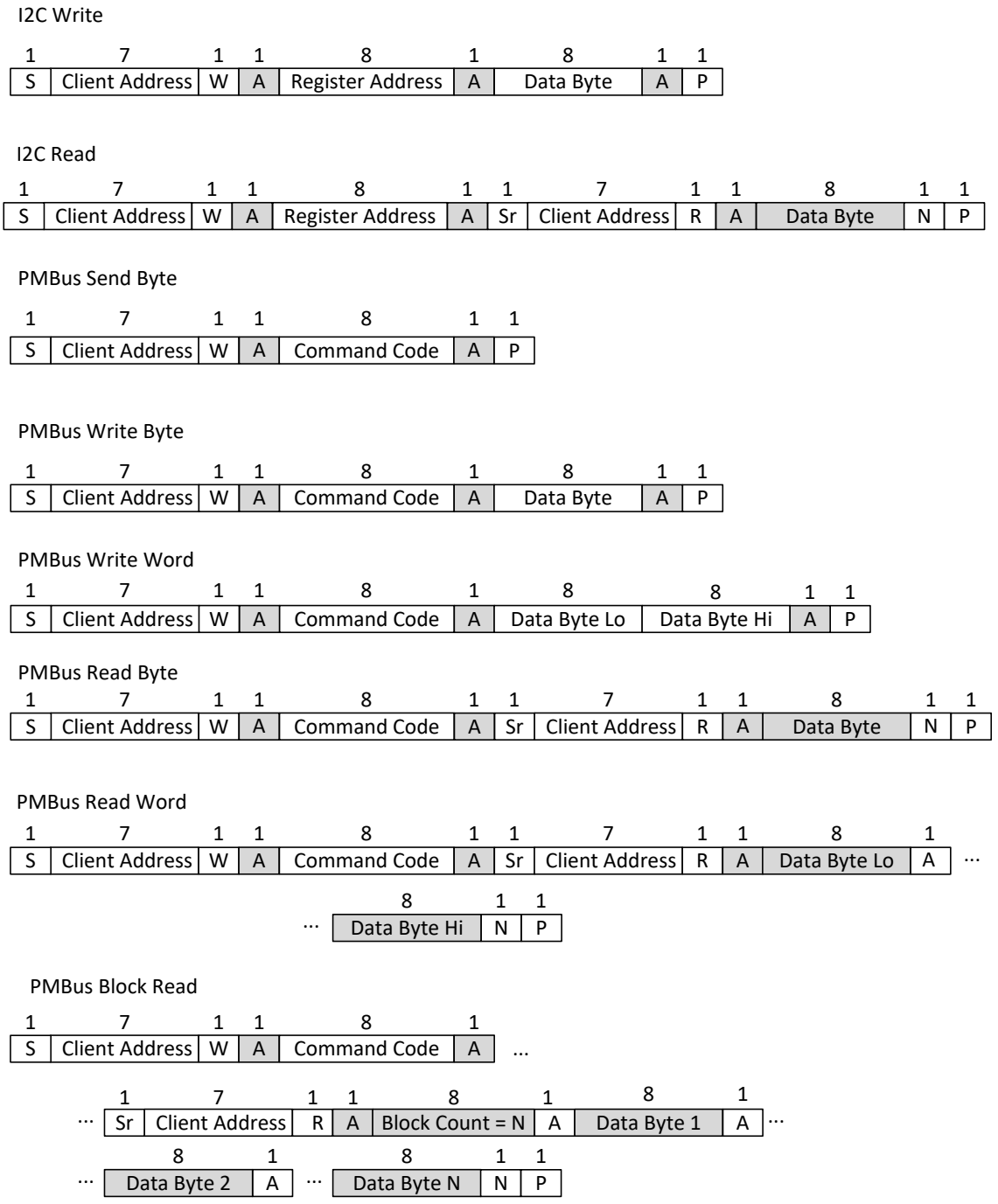
9. Programming the OTP

1. Write all registers with desired values and save these values for later comparison.
2. Pulle the EN pin low (or high, depending on the polarity value set in the ON_OFF_CONFIG register) to disable switching.
3. Read register USER_OTP_POINTER (0xF2) to determine the number of remaining writes.
4. If there is a bank remaining, apply 7.5V (±250 mV) to the VIN pin. If there is not a bank remaining, the part cannot be written with new values.
5. Write a 0 then a 1 to the register BURN_OTP (0xC9), bit[1].
6. Read the STATUS register (0xF3) and check bit[1]. If the bit is set, the write was successful. If not, the write was not successful.
7. If the write was successful, power cycle the part.
8. Read all programmed registers and compare to the values saved in step 1.
9. If steps 6 or 8 fail, repeat the process.
10. If there is a second failure of steps 6 or 8, discard the part.

10. Protocols

S = Start Bit	W = Write Bit, 0	White Background = Sent by Host
P = Stop Bit	R = Read Bit, 1	
A = ACK	Sr = Repeated Start Bit	Grey Background = Sent by MCPF1525M06
N = NACK		

Figure 10-1. I²C Protocols



11. Packaging Information

Package Marking Information

Package type:

MCPF
1525
NNNNNN
YYWW

Example:

MCPF
1525
23F5E1
2545

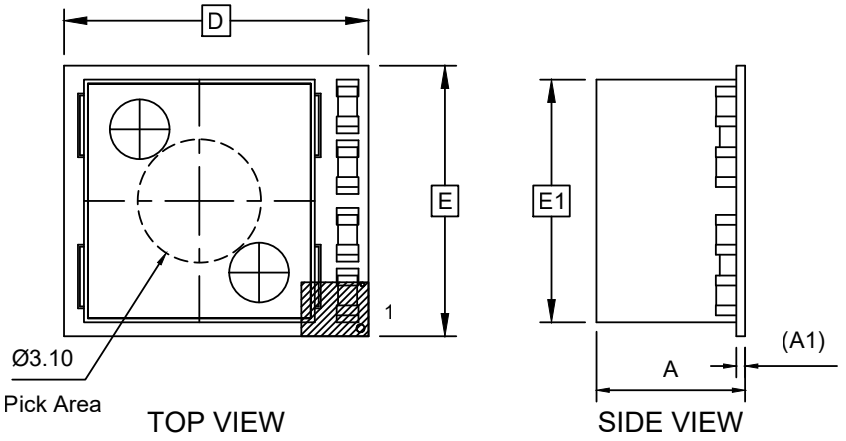
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

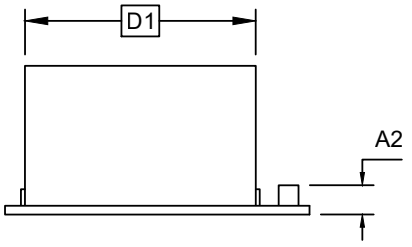
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

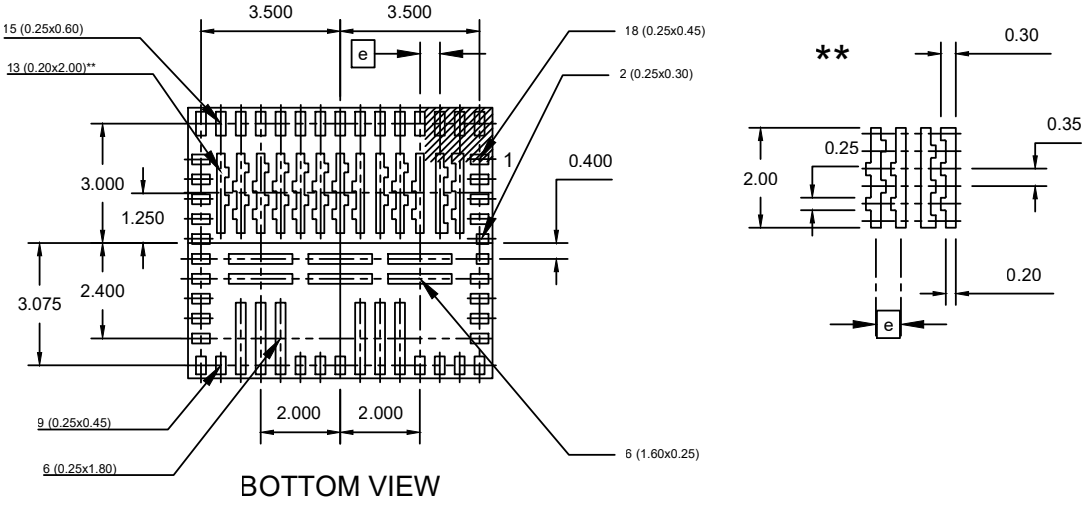
Package Outline Drawing

69-Lead Extra Thick Land Grid Array-SIP (8ZW) 7.65x6.8x4.02mm[B2LGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



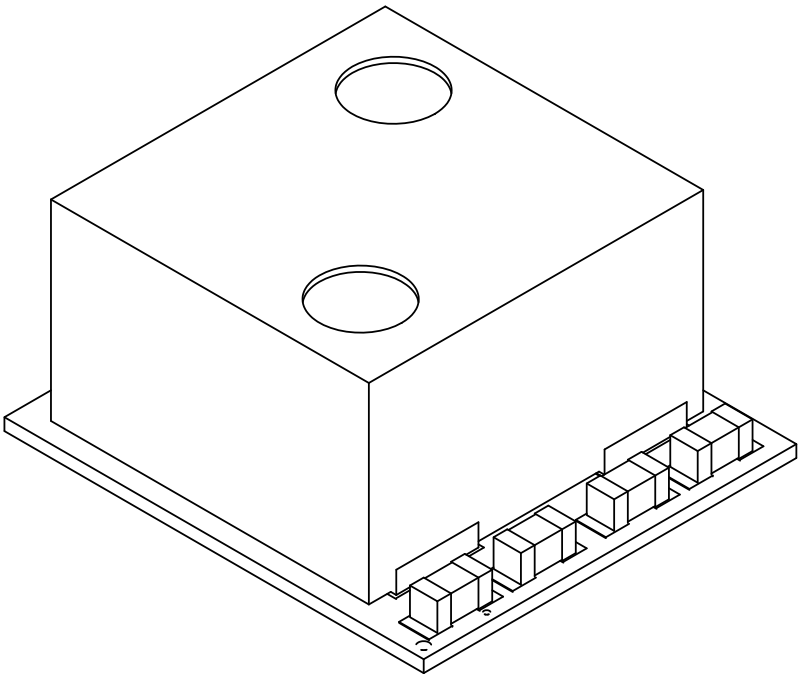




Microchip Technology Drawing C04-00678 Rev A Sheet 1 of 2

69-Lead Extra Thick Land Grid Array-SIP (8ZW) 7.65x6.8x4.02mm[B2LGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



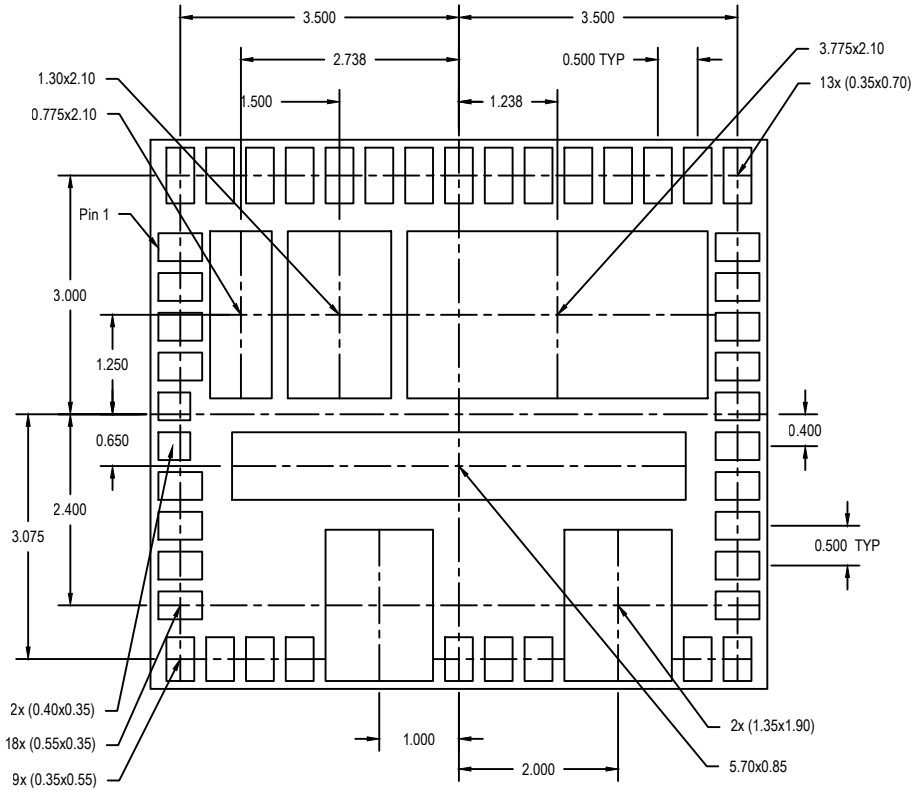
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		69	
Pitch	e		0.50 BSC	
Overall Height	A	3.62	3.82	4.02
Package Base	A1		0.33 REF	
Component Height from Bottom	A2	0.73	0.93	1.13
Overall Length	D		7.65 BSC	
Inductor Length	D1		6.10 BSC	
Overall Width	E		6.80 BSC	
Inductor Width	E1		6.00 BSC	

Notes:

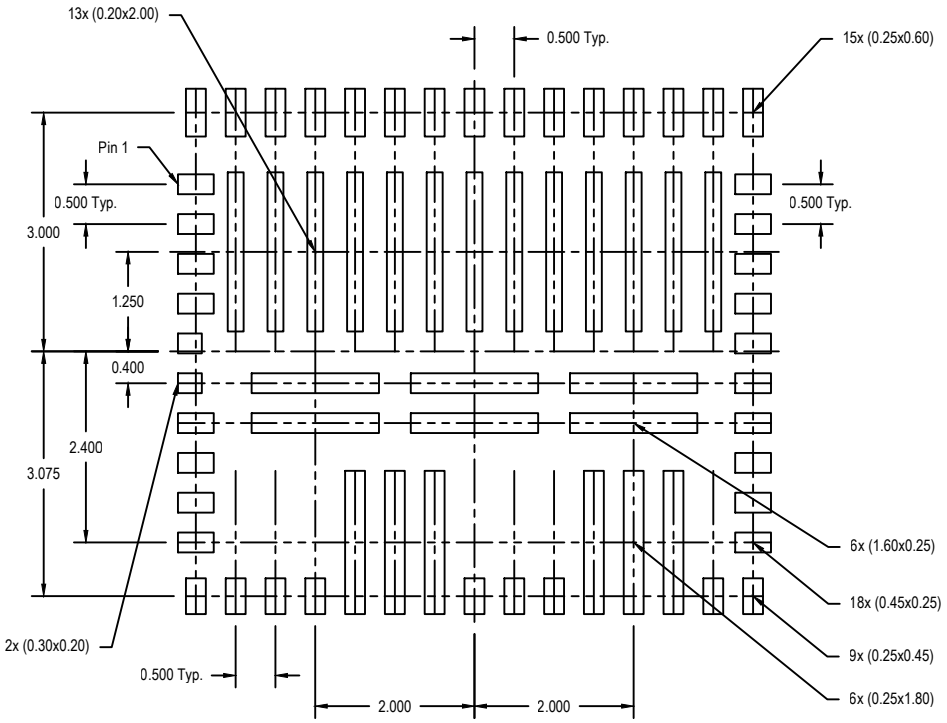
1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerances, is for information purposes only.

Microchip Technology Drawing C04-00678 Rev A Sheet 2 of 2

69-Lead Extra Thick Land Grid Arrray-SIP (8ZW) 7.65x6.8x4.02mm[B2LGA]



Solder Mask



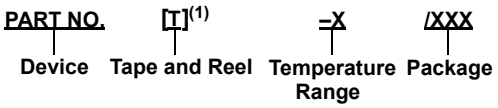
Solder Stencil

12. Revision History

Doc. Rev.	Date	Section	Comments
A	January 2026	—	Initial release of MCPF1525M06 as Microchip document DS60001915A.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.



Device:	MCPF1525M06: 16V, 25A Stackable Switching Buck Regulator Module	
Tape & Reel Option(1):	Blank	= Tube
	T	= Tape and Reel
Temperature Range:	E	= −40°C to +125°C (Extended)
Package:	8ZW	= Extra Thick Land Grid Array (B2LGA), 69-Pin,7.65 × 6.8 × 3.9 mm

Examples:

- MCPF1525M06T-E/8ZW: 16V, 25A Stackable Switching Buck Regulator Module, Tape and Reel, Extended Temperature, B2LGA 69-Pin Package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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ISBN: 979-8-3371-2677-7

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