16V, 35A Switching Buck Regulator Module

MIC45M235 Switching Buck Regulator Module

Description

The MIC45M235 is a 16V rated, 35A Power Module that combines a PWM controller, a MOSFET driver with power MOSFETs, an inductor, and passives into a compact Land Grid Array (LGA) package. This power solution requires few external components while maintaining the ability to adjust key parameters to meet specific design requirements. It provides a highly efficient solution optimized for 12V input applications and low-voltage outputs. It has built-in protection features including pre-biased start-up, soft-start protection, overvoltage protection, thermally compensated overcurrent protection with hiccup mode, and thermal shutdown with auto-recovery.

Features

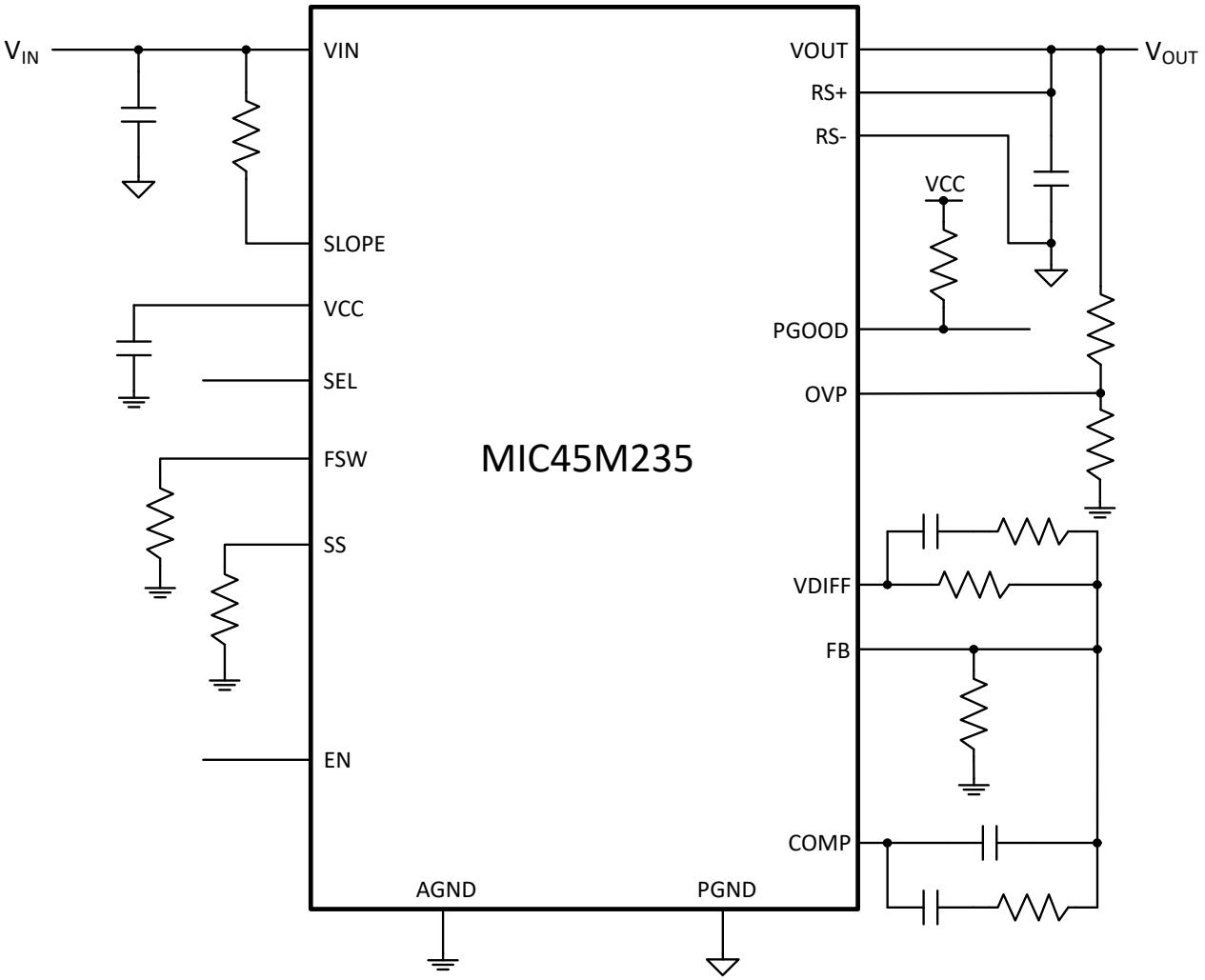
- POL Module With Integrated Inductor
- 35A Continuous Output Rating
- High Efficiency
- Differential Remote Voltage Sensing
- 4.5V to 16V Input Voltage Range
- Adjustable Output From 0.6V to 3.46V
  - Recommended range: 0.6V to 1.8V
- Enable Input
- Programmable Valley Current Mode or Voltage Mode Control
- Adjustable Switching Frequency: 200 kHz to 2 MHz
  - Recommended range: 300 kHz to 700 kHz
- Power Good Output
- Overvoltage and Overcurrent Protection
- Thermal Shutdown With Hysteresis
- Programmable Soft Start
- Supports Start-up Into Pre-biased Output
- −40°C to 85°C Ambient Temperature Range
- 11 × 17 × 6.46 mm LGA Package

Applications

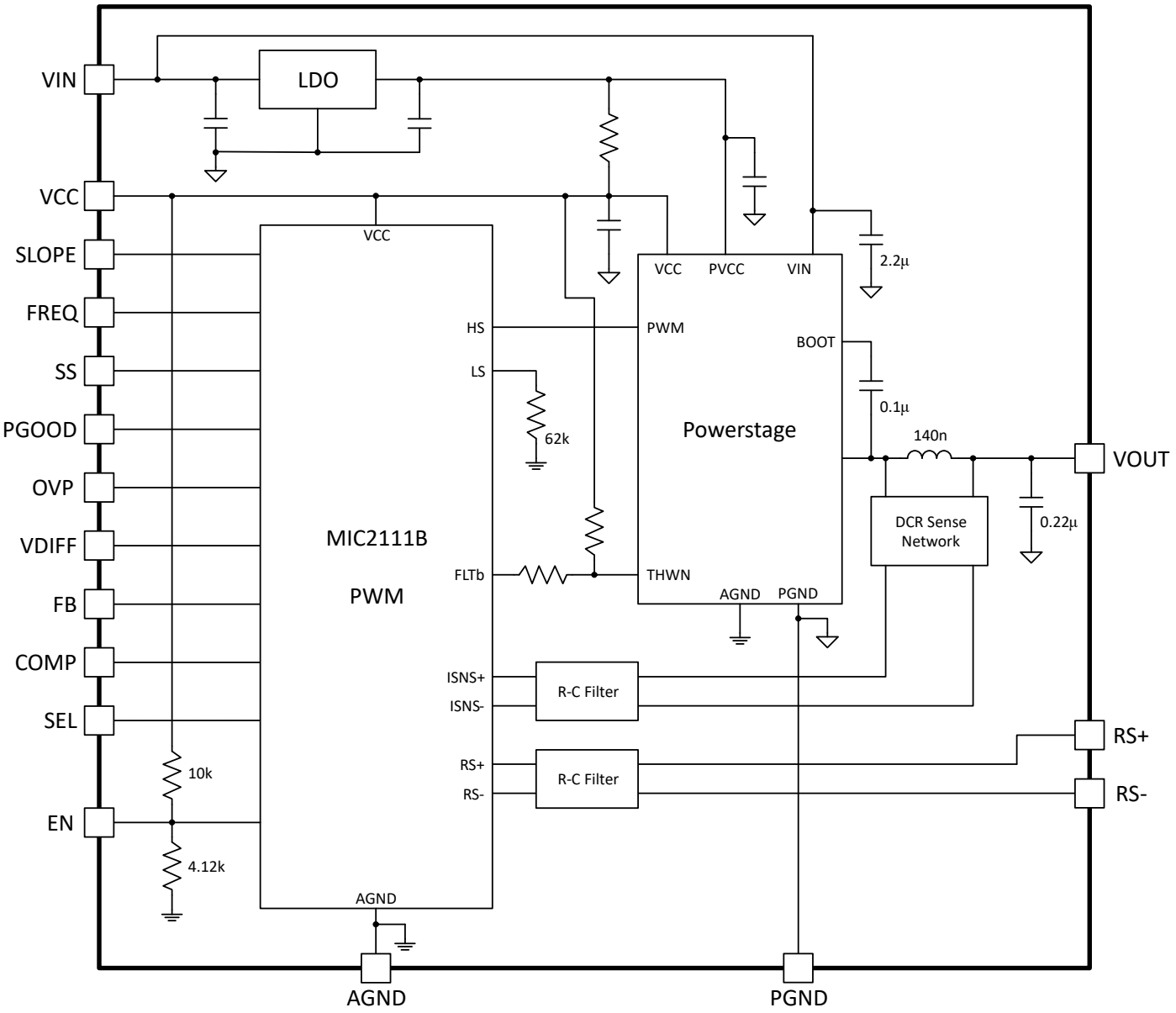
- Telecommunications and Networking
- Data Centers
- Storage
- Industrial
- Distributed Point of Load
- Computing Peripherals

Typical Application Circuits

Figure 1. Voltage Mode Control Typical Configuration



Block Diagram

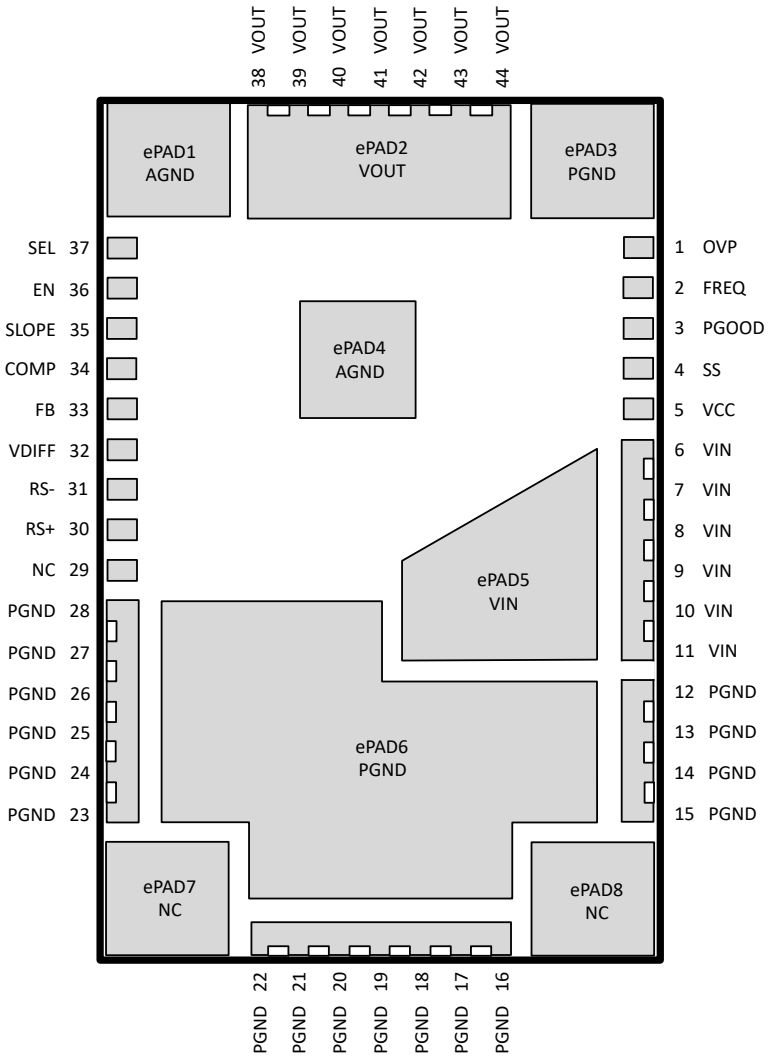


1. Pin Configuration

Pin Number	Name	Pin Description
1	OVP	Output Overvoltage Protection pin. Connect a resistor divider from VOUT to AGND to set the OVP threshold. The internal reference for the OVP comparator is 0.6V.
2	FREQ	Frequency Programming Input pin. Connect a resistor from the FREQ pin to AGND to set the switching frequency.
3	PGOOD	Open-Drain Power Good Output pin. PGOOD is pulled to ground when the output voltage is below 90% of the target voltage. Pull-up to VCC through a resistor to set logic high level when the output voltage is above 92% of the target voltage.
4	SS	Soft Start Adjustment pin. Connect a resistor from the SS pin to AGND to adjust the soft start time.
5	VCC	5V LDO Output pin. Bias supply for the PWM controller and also PVCC internally for Powerstage gate drive. Connect a minimum 0.1 µF low-ESR ceramic capacitor from VCC to AGND.
6-11, ePAD5	VIN	Power Input Pins. Apply the input voltage between these pins and GND pins. Place input decoupling capacitance directly between the VIN and PGND pins.
12-28, ePAD3, ePAD6	PGND	Power Ground pin. PGND is the return path for the low-side MOSFET current and for the low-side MOSFET driver. Connect all the PGND pins together and connect to the power ground plane.
29, ePAD7, ePAD8	NC	NC pins; leave floating.
30	RS+	Remote Output Voltage Sense pin. The non-inverting input to the remote sense amplifier. Internal filter consists of series 10Ω and 10 pF connected from RS+ to RS−.
31	RS-	Remote Output Ground Sense pin. The inverting input to the remote sense amplifier. Internal filter consists of series 10Ω and 10 pF connected from RS− to RS+.
32	VDIFF	Output of differential amplifier. Connect a resistor divider from VDIFF to AGND, connecting midpoint to FB, to set the output voltage. It is recommended to add 100 pF filtering cap from VDIFF to AGND.
33	FB	Output Voltage Feedback pin. Connect midpoint of resistor divider from VDIFF to AGND to the FB pin.
34	COMP	Transconductance Amplifier Output. Connect compensation components to this pin to adjust Module frequency response and stability.
35	SLOPE	Slope Compensation pin. Adjust slope compensation with a resistor tied to VIN.
36	EN	Active-High Enable Input pin. CMOS compatible logic signal to enable/disable the Module. Logic high enables the Module.
37	SEL	Control Mode Selection pin. Connect this pin to AGND for valley current-mode operation. Leave this pin open for voltage-mode control operation.
38-44, ePAD2	VOUT	Power Output Pins. Apply output load between these pins and PGND pins. Place output decoupling capacitance directly between these pins and PGND pins.
ePAD1, ePAD4	AGND	Analog Ground pin. Reference node for all control logic circuits inside the MIC45M235. Connect AGND to PGND at one point.

1.1. Package Type

Figure 1-1. 5JW LGA Package, Bottom View



2. Functional Description

2.1. Overview

The MIC45M235 is a high-efficiency, single output DC/DC Buck Converter Module. It can provide up to 35A continuous output current with few external components. The Module provides precisely regulated output voltages adjustable from 0.6V to 3.3V over a 4.5V to 16V input voltage range.

The Module integrates a MIC2111B PWM controller, a power stage, an inductor, protection circuitry, a 5V regulator for bias, and other supporting discrete components. The MIC45M235 can support switching frequencies from 200 kHz to 2 MHz but is optimized to run in a range from 300 kHz to 700 kHz, depending on the output voltage.

The MIC45M235 is a single-phase step-down Module that can be operated in two different constant frequency control architectures – valley current mode or voltage mode control.

The Module implements overcurrent protection by sensing current via inductor DCR-sensing. This sensed current is scaled and temperature compensated and fed back to the PWM controller to implement hiccup mode current limit.

The MIC45M235 has a dedicated pin for Overvoltage Protection (OVP), typically protecting against an open or shorted feedback loop.

The Module has thermal shutdown when the junction temperature of the power stage hits 150°C, and it is released when the temperature falls below 130°C.

Startup and shutdown of the MIC45M235 are managed by the EN and SS pins. Pulling the EN pin below 1.2V forces the Module into a shutdown state. The SS pin is used to program the soft-start time of the output voltage ramp during start-up.

High efficiency at light loads is enhanced with the built-in pulse-skipping mode, also referred to as Discontinuous Conduction Mode (DCM).

2.2. Operation

The MIC45M235 is a highly integrated single-phase step-down DC-DC converter. It is easy to operate and integrate into various systems.

2.2.1. Step Down Ratios and Minimum t_{ON}, Minimum t_{OFF}

There are restrictions in the input voltage (V_{IN}) to output voltage (V_{OUT}) step-down ratio that can be achieved for a given V_{IN}, V_{OUT} and switching frequency (f_{SW}). The minimum on-time, $t_{ON(MIN)}$, limits the shortest time duration that the Module is capable of turning on the top MOSFET. The absolute minimum V_{OUT} is 0.6V based on the internal bandgap reference of the PWM controller. At very low duty cycles and higher f_{SW}, the $t_{ON(MIN)}$ of 40 ns (typical) can impact the minimum achievable V_{OUT}. The equation accounts for minimum V_{OUT} including the minimum t_{ON} and it is detailed below. Equation 2-1 accounts for inefficiencies in the circuit due to MOSFET conduction losses, but ignores inductor DCR and PCB losses.

Equation 2-1.

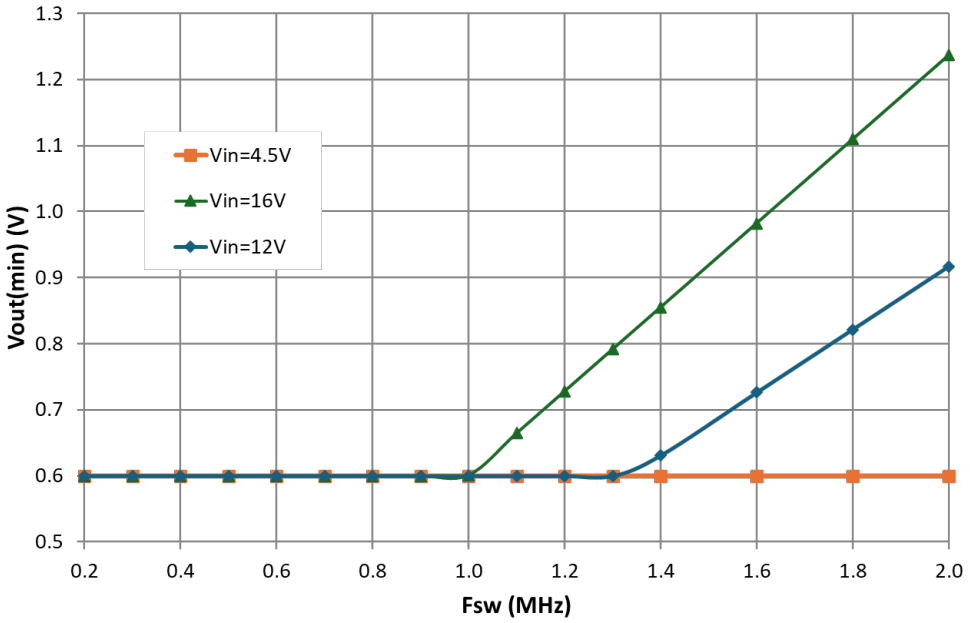
$$V_{OUT(MIN)} = t_{ON(MIN)} \cdot f_{SW} \cdot (V_{IN} - V_{UFET} + V_{LFET}) - V_{LFET}$$

Where:

- V_{UFET}: voltage drop across Upper MOSFET
- V_{LFET}: voltage drop across Lower MOSFET

Figure 2-1 plots $V_{OUT(MIN)}$ as a function of f_{SW} for various input voltages based on Equation 2-1. Within the recommended f_{SW} range of 300-700 kHz there should be no impact on minimum VOUT due to $t_{ON(MIN)}$.

Figure 2-1. $V_{OUT(MIN)}$ Versus Switching Frequency and Input Voltage



Conversely, the minimum OFF-time of 100 ns is required for higher duty cycles and theoretically could impact the maximum achievable V_{OUT}. However, the MIC45M235 maximum V_{OUT} is 3.46V and the $t_{OFF(MIN)}$ does not restrict $V_{OUT(MAX)}$.

2.2.2. Switching Frequency

The MIC2111B has an internal oscillator and the frequency can be set through an external resistor connected from the FREQ pin to AGND. The switching frequency can be programmed from 200 kHz to 2 MHz using Equation 2-2:

Equation 2-2.

$$R_{FREQ} = \frac{10^5}{f_{SW}}$$

The following table is also a useful quick reference, with the recommended f_{SW} range highlighted in red.

Table 2-1. Programming the Switching Frequency

Desired f_{SW} (kHz)	R_{FREQ} (kΩ)
200	500
300	333.3
400	250
500	200
600	166.7
700	142.9
1000	100
2000	50

Please note that standard resistor values may not exactly match the R_{FREQ} values in the table above.

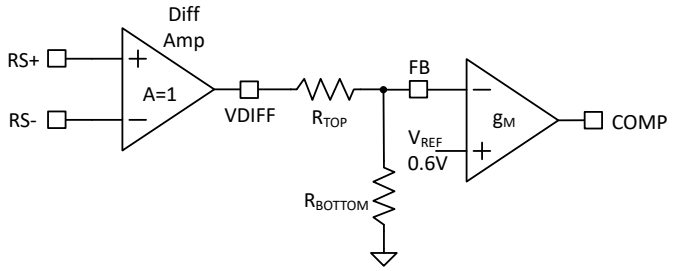
2.2.3. V_{OUT} Setting

Equation 2-3 and Figure 2-2 describe the relationship between the resistor divider ratio and the output voltage of the MIC45M235. The divider resistors should be in the tens of kΩ range.

Equation 2-3.

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right)$$

Figure 2-2. Resistor Divider Programming of Output Voltage



2.2.4. Recommended Operational Ranges

The MIC45M235 has been designed to optimally run in the following set of operating conditions:

- V_{IN} range: 10-14V
- V_{OUT} range: 0.6-1.8V
- f_{SW} range: 300-700 kHz
- I_{OUT} range: 0-35A

Other operating conditions may be supported; the user should take careful consideration when doing so.

2.2.5. Internal LDO

The MIC45M235 integrates an MIC5219 low-dropout (LDO) regulator for internal 5V bias, enabling single-input supply operation. The 5V bias is used for both powerstage gate drive (PVCC, internal only) and PWM controller and powerstage bias supply (VCC, internal and brought out to an external pin). The Modules incorporates internal decoupling of both VCC and PVCC. External decoupling of the VCC pin is also recommended.

2.2.6. Startup

The precision EN pin is used to enable or disable the MIC45M235. The typical threshold is 1.2V. When the voltage at EN rises above the threshold, the Module is enabled and starts normal operation after initialization of the internal oscillator, references, current-limit settings, and the soft start period. The MIC45M235 has initialization delay of 250 µs before the PWM output starts.

When the voltage at EN drops 50 mV or more (hysteresis) below the threshold voltage, then the internal controller circuits of the PWM controller are turned off. It is possible to use the EN pin for sequencing multiple power supplies along with Power Good (PG) pin. An external RC delay may be added to achieve sequencing.

The MIC45M235 has an internal resistor divider on the EN pin, as shown in the Block Diagram. This provides a nominal Under-Voltage Lockout (UVLO) level of VCC = 4.1V with ~15 mV of hysteresis.

The Module incorporates digital Soft Start (SS) to avoid high inrush current. Soft start time can be programmed with an external resistor connected from the SS pin to GND. The table below illustrates resistor values and soft start time.

Table 2-2. Soft Start Programming

SS resistor	Soft Start (µs)	SS resistor	Soft Start (µs)
6.19 kΩ	64	105 kΩ	3072
19.1 kΩ	128	118 kΩ	4096
30.9 kΩ	256	130 kΩ	6144
44.2 kΩ	512	143 kΩ	8192
56.2 kΩ	768	154 kΩ	16384
68.1 kΩ	1024	169 kΩ	24576
80.6 kΩ	1536	182 kΩ	32768
93.1 kΩ	2048	Open	2048

2.2.7. Power Good

The Power Good (PGOOD) pin is an open-drain output. An external pull-up resistor is required between PGOOD and an external voltage (typically VCC is used). When the feedback voltage, V_{FB}, rises above the PGOOD threshold (92% typical of V_{REF}; V_{REF} = 0.6V), the PGOOD output is pulled high after a delay of ~200 µs.

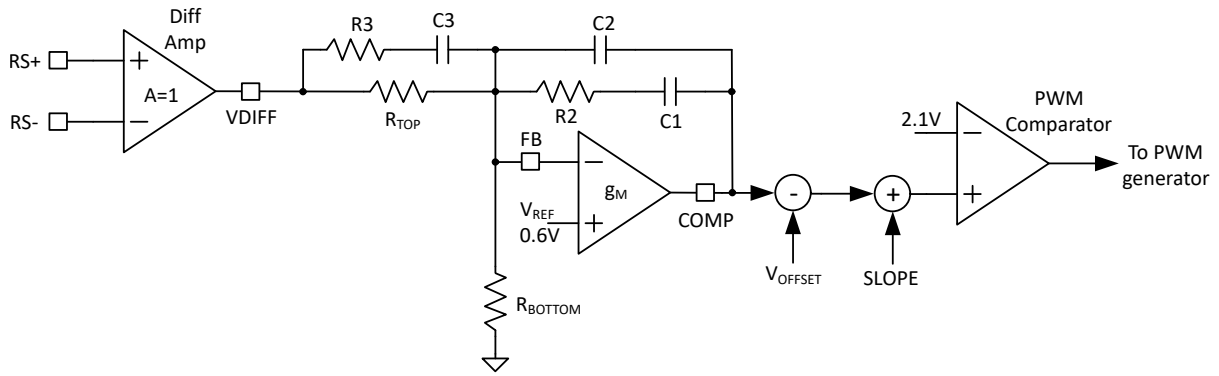
2.2.8. Control Modes and Compensation

The control architecture is pin-programmable using the SEL pin. It can be either voltage mode control or valley current mode control.

2.2.8.1. Voltage Mode Control

The MIC45M235 can be configured in Voltage Mode (VM) control by leaving the SEL pin floating. As detailed in Figure 2-3, an internal transconductance amplifier produces an integrated error voltage at COMP that helps to provide high DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and a ramp generator. The VM ramp is generated by connecting a resistor between VIN and the SLOPE pin. The VM control scheme uses leading-edge modulation, as detailed in Figure 2-4. The PWM comparator initiates the PWM ON-time once the non-inverting input to the PWM comparator reaches a 2.1V threshold. On the rising edge of an internal clock, the PWM signal is terminated. Control-loop compensation is external for flexibility; type 3 compensation is recommended for VM control as detailed in Figure 2-3.

Figure 2-3. Voltage Mode Configuration and Compensation



In voltage mode, the SLOPE pin is used to generate the ramp which gets summed into the error signal (COMP minus ~150 mV offset). The VM ramp at the PWM comparator non-inverting input is implemented by selecting the following R_{SLOPE} resistor value from SLOPE to VIN:

Equation 2-4.

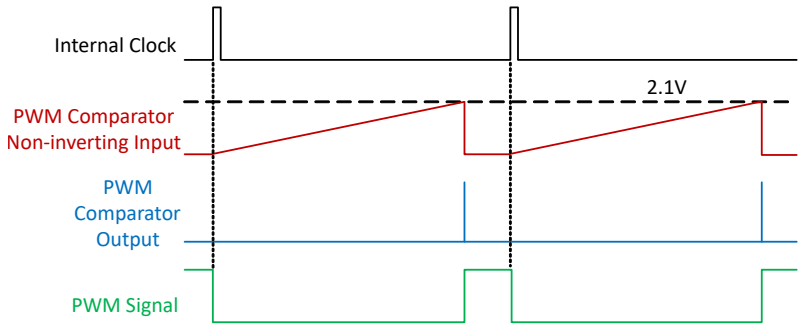
$$R_{SLOPE} = \frac{K_{SLOPE} \cdot t_{OFF} \cdot (V_{IN} - V_{OUT})}{RAMP_{P-P}}$$

Where:

- K_{SLOPE} = 1.33 × 10^{10} Ω/s
- t_{OFF} = OFF-time of upper MOSFET = T • (1 – V_{OUT}/V_{IN})
- T = Switching period ($1/f_{SW}$)
- V_{IN} = System input voltage
- V_{OUT} = Output voltage
- $RAMP_{P-P}$ = peak-to-peak voltage of summed ramp on modified COMP signal

Setting $RAMP_{P-P}$ = 1V is a good setting for the MIC45M235. Figure 2-4 details typical VM control waveforms.

Figure 2-4. Leading-Edge Voltage Mode Modulation Waveforms



2.2.8.2. Voltage Mode Control Compensation

To choose the appropriate compensation components in VM control, we must first determine the output filter resonant frequency, F_{LC}, using Equation 2-5 and the ESR zero of C_{OUT}, F_{ESR}, using Equation 2-6:

Equation 2-5.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}$$

Where:

- L_{OUT} = Output filter inductance, which is 140 nH
- C_{OUT} = Output filter capacitance

Equation 2-6.

$$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} . ESR}$$

Where:

- ESR = equivalent series resistance of the output filter capacitance

Referring to Figure 2-3, the compensation network consists of components R_{TOP}, R2, R3, C1, C2, C3 and the g_M amplifier. With sufficiently high impedances of the compensation components, the g_M

amplifier can be used exactly as an operational amplifier (error amp). Two good guidelines to meet the high impedance advice:

$R2 >> 1/g_M$

R_{TOP} // R_{BOTTOM} // R3 >> $1/g_M$

The goal of the compensation network is to provide a closed loop transfer function with a "high" crossover frequency with sufficient phase margin. A good target for crossover frequency is 1/10th the Module's switching frequency and a good target for phase margin is 45 degrees or higher.

Use the following procedure and Equations 2-7 to 2-10 to design the VM compensation:

1. Place 1st Zero (F_{Z1}) approximately 50-75% below F_{LC}
2. Place 2nd Zero (F_{Z2}) approximately at F_{LC}
3. Place 1st Pole (F_{P1}) approximately at F_{ESR}
4. Place 2nd Pole (F_{P2}) approximately at 50% of f_{SW}

Equation 2-7.

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1}$$

Equation 2-8.

$$F_{Z2} = \frac{1}{2\pi \cdot (R_{TOP} + R_3) \cdot C_3}$$

Equation 2-9.

$$F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)}$$

Equation 2-10.

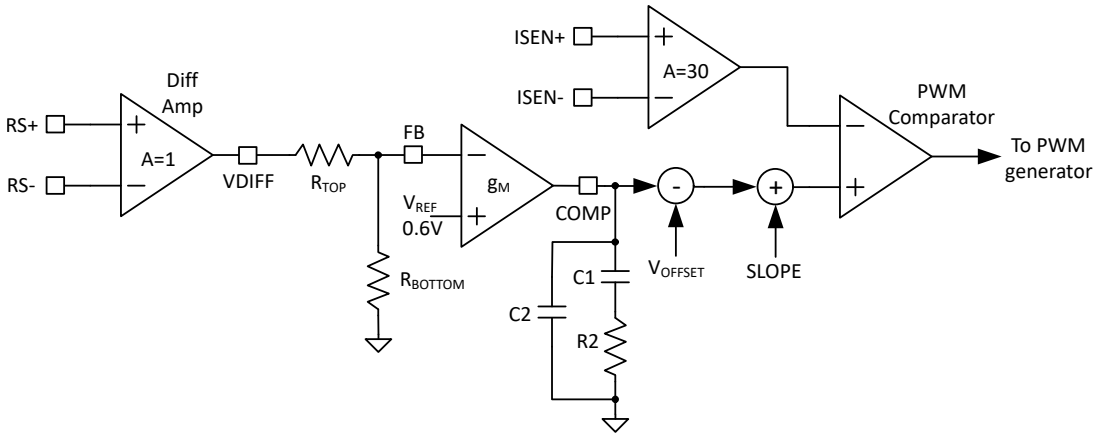
$$F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3}$$

It is recommended to check both the frequency response (Bode plot) and time-domain response (load step transient response). It may be necessary to adjust the compensation components to optimize the solution.

2.2.8.3. Valley Current Mode Control

The MIC45M235 can be configured in valley current-mode (VCM) control by grounding the SEL pin. When the MIC45M235 is programmed to VCM control architecture, the inductor current is sensed by the voltage drop measured across the DCR of the inductor. The current is sensed during the off period of the switching cycle. It is filtered (series 100Ω and 100 pF to AGND on both ends of the differential signal) and is conditioned by the current sense amplifier, which has a gain of 30 V/V. The output signal of the current sense amplifier is compared with the current programmed by the g_M amplifier to determine the correct duty cycle. Slope compensation is added via a resistor between VIN and the SLOPE pin. This slope compensation ramp is then added to comp signal to avoid sub-harmonic oscillations for duty cycles of less than 50%, see Figure 2-5.

Figure 2-5. Valley Current Mode Configuration and Compensation



In VCM control, the SLOPE pin is used for slope compensation. The MIC45M235 applies slope compensation dependent on V_{IN}, V_{OUT}, and output filter inductance by a single resistor connected between VIN and the SLOPE pin.

Equation 2-11.

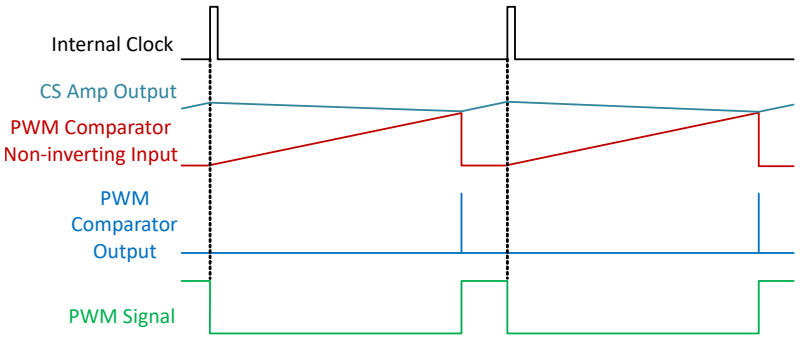
$$R_{SLOPE} = \frac{K_{SLOPE} \cdot L}{SF \cdot A_{ISENAMP} \cdot DCR \cdot AF}$$

Where:

- SF = Slope Factor
- K_{SLOPE} = 1.33×10^{10} Ω/s
- L = Output filter inductance, which is 140 nH
- $A_{ISENAMP}$ = Current Sense Amplifier gain, which is 30
- DCR = DC Resistance of Output Inductor, which is 0.3 mΩ
- AF = attenuation factor of temperature-compensated DCR sensing network, which is 0.745

Set SF = 1 for "1x slope compensation," which sets the injected slope equal to the slope at the output of the CS amplifier during the upper MOSFET ON-time. Set SF less than 1 for reduced amount of slope compensation, and vice-versa. See Figure 2-6 for key VCM waveforms.

Figure 2-6. Valley Current Mode Modulation Waveforms



2.2.8.4. Valley Current Mode Control Compensation

Valley current mode control regulates the duty cycle to deliver the "valley" inductor current required to control the output voltage. The valley current of the inductor is the current at the end of the OFF-time, which is the time when the lower MOSFET is conducting. Because the inductor current is

regulated, the LC resonance in the output filter is eliminated and the inductor can be modeled as an ideal current source. This results in reduced phase shift and requires less elaborate compensation than voltage-mode control.

A pole (F_P) is formed by the load resistance and output capacitance as shown in Equation 2-12. The ESR zero is the same as in VM control (Equation 2-6 repeated here, shown as Equation 2-13):

Equation 2-12.

$$F_P = \frac{1}{2\pi \cdot R_L \cdot C_{OUT}}$$

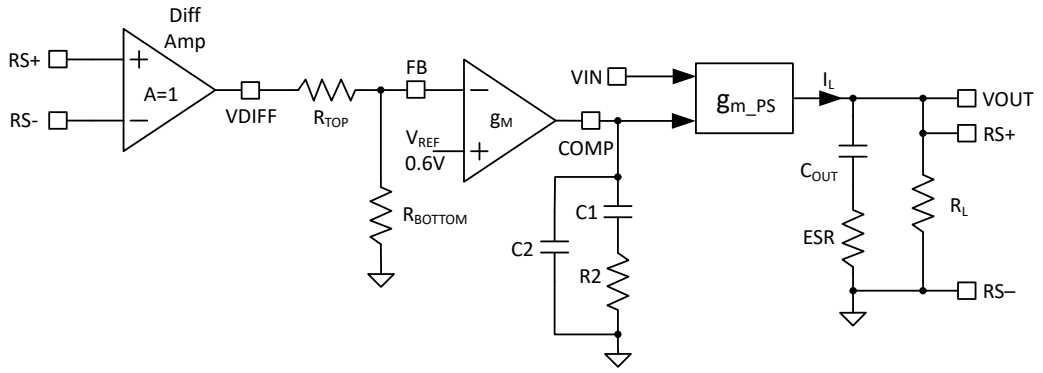
Equation 2-13.

$$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$$

A simple series R and C (R2 and C1 in Figure 2-5) is all that is needed to have a stable, high-bandwidth loop in applications when ceramic capacitors are used for output filtering. When using other types of capacitors, due to the higher capacitance and ESR, the ESR zero may be lower than the desired closed-loop crossover frequency. In this case, an additional compensation capacitor from COMP to GND (C2 in Figure 2-5) is necessary to cancel this ESR zero. If not needed for stability, C2 is generally recommended to mitigate high frequency noise. In this case, select C2 to place the resulting pole at approximately 10x the desired crossover frequency.

As a simple first-order approximation, the VCM controlled buck power stage can be modeled as a voltage-controlled current source, feeding the output capacitor and load. The inductor current state variable is removed and the power stage transfer function from COMP to the inductor current is modeled as a transconductance (g_{M_PS}). The simplified model of the control loop is shown in Figure 2-7.

Figure 2-7. Simplified Small Signal Model of Valley Current Mode Loop



The loop gain in the frequency domain is defined by Equation 2-14.

Equation 2-14.

$$H(f)_{LOOP} = H(f)_{CO} \cdot H(f)_{COMP}$$

Where:

- $H(f)_{CO}$ = Control-to-output transfer function
- $H(f)_{COMP}$ = Compensator transfer function

Equation 2-15 provides an estimate of the control-to-output transfer function.

Equation 2-15.

$$H(f)_{CO} = g_{M\_PS} \cdot R_L \cdot \frac{1 + s \cdot C_{OUT} \cdot ESR}{1 + s \cdot C_{OUT} \cdot R_L}$$

Where:

- g_{M_PS} = power stage
- g_M = 110 A/V

The power stage g_M, g_{M_PS}, is defined as the change in output load current divided by the change in COMP voltage. It is not an absolute number under all conditions; 110A/V is a typical number to use for the MIC45M235 recommended operational conditions.

As shown in Figures 2-5 and 2-7, a compensation network comprised of C1, R2, and C2, is used to stabilize the loop, and its gain is referred to as $H(f)_{COMP}$. Equation 2-16 provides the compensator transfer function.

Equation 2-16.

$$H(f)_{COMP} = \left(g_M \cdot \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}}\right) \cdot \frac{1}{s \cdot C_1} \cdot \frac{1 + s \cdot C_1 \cdot R_2}{1 + s \cdot C_2 \cdot R_2}$$

Equation 2-16 assumes C2 << C1. Equations 2-17 and 2-18 define the compensator pole and the zero.

Equation 2-17.

$$F_{Zcomp} = \frac{1}{2\pi \cdot C_1 \cdot R_2}$$

Equation 2-18.

$$F_{Pcomp} = \frac{1}{2\pi \cdot C_2 \cdot R_2}$$

Substituting Equations 2-15 and 2-16 into Equation 2-14 gives us the total loop gain. If we design the compensating pole and zero to cancel the load pole and zero, we arrive at an overall loop gain as described by Equation 2-19.

Equation 2-19.

$$H(f)_{LOOP} = g_{M\_PS} \cdot \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \cdot g_M \cdot \frac{R_L}{s \cdot C_1}$$

Equating Equations 2-12 and 2-17 also gives us Equation 2-20.

Equation 2-20.

$$\frac{R_L}{C_1} = \frac{R_2}{C_{OUT}}$$

Subbing Equation 2-20 into Equation 2-19, and noting that at the crossover frequency, $s = 2\pi \times F_C$ and $H(f)_{LOOP} = 1$, Equation 2-19 can be rearranged to Equation 2-21 to calculate the estimated crossover frequency.

Equation 2-21.

$$F_C = g_{M\_PS} \cdot \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \cdot g_M \cdot \frac{R_2}{2\pi \cdot C_{OUT}}$$

Summarizing, use the following procedure and Equations 2-22 to 2-24 to design the VCM compensation:

1. Place the Zero (F_{Zcomp}) at approximately the same frequency as the load Pole (F_P).
2. Place the Pole (F_{Pcomp}) at approximately the same frequency as the ESR Zero (F_{ESR}).

Equation 2-22.

$$R_2 = \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \cdot \frac{2\pi \cdot C_{OUT} \cdot F_C}{g_{M\_PS} \cdot g_M}$$

Equation 2-23.

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot F_P}$$

Equation 2-24.

$$C_2 = \frac{1}{2\pi \cdot C_{OUT} \cdot F_{ESR}}$$

2.2.9. DCM Operation

The MIC45M235 will run in Discontinuous Conduction Mode (DCM), or pulse-skip mode, for improved light efficiency. To avoid discharging the output during this light-load mode, the smart power stage zero current detector disables the low-side FET once inductor current reaches zero. The MIC45M235 generates the next PWM signal based on COMP voltage, causing DCM operation.

2.2.10. Protections

2.2.10.1. Overcurrent Limit

The MIC45M235 has internal Overcurrent Protection (OCP) set at a nominal 45A load current. It employs thermally-compensated inductor DC Resistance (DCR) sensing and operates in hiccup protection mode. The MIC45M235 uses a proprietary hiccup mode current-limit algorithm to avoid saturation of inductor. An internal counter increments by two in each cycle overcurrent is detected, and decrements by one each cycle when the current is not over the limit. When the counter reaches 16, the part will shut down due to hitting current limit and will wait for 8 ms before initiating a soft start.

2.2.10.2. Overvoltage Protection

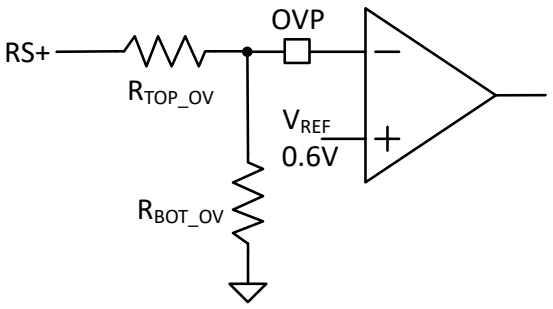
The MIC45M235 has a dedicated pin for Overvoltage Protection (OVP), typically protecting against an open feedback loop or V_{FB} short-to-GND. The OVP pin senses the output voltage through an external voltage divider. If this voltage is higher than V_{REF}, the overvoltage protection engages and the Module is latched off. It is required to cycle either VCC (via VIN) or EN to re-enable the Module.

The OVP level, V_{OUT_OV}, is programmed through a resistive divider at the OVP pin as shown in Equation 2-25 and Figure 2-8. The divider resistors should be in the tens of kΩ range.

Equation 2-25.

$$V_{OUT\_OV} = 0.6V \cdot \left(1 + \frac{R_{TOP\_OV}}{R_{BOT\_OV}}\right)$$

Figure 2-8. OVP Programming



2.2.10.3. Thermal Shutdown

The powerstage temperature is internally monitored and the MIC45M235 is disabled if it exceeds ~150°C. There is approximately 15°C of thermal hysteresis and the MIC45M235 will attempt to restart when the temperature cools to ~135°C.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Parameter(s)	Symbol	Min.	Max.	Unit
VIN to PGND		−0.3	20	V
VCC to AGND		−0.3	6	V
EN, SS, FREQ, OVP, RS+, RS−, FB to AGND		−0.3	VCC + 0.3V	V
SLOPE to AGND		−0.3	20	V

⚠ WARNING Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2. Recommended Operating Conditions

Parameter(s)	Symbol	Min.	Max.	Unit
VIN		4.5	16	V
VCC		4.5	5.5	V
VOUT		0.6	3.3	V
EN		0	VCC	V
Ambient Temperature (T_A)		−40	85	°C

3.3. DC/AC Characteristics

V_{IN} = 12V; V_{OUT} = 1.0V; f_{SW} = 400 kHz; T_A = +25°C, unless noted. **Boldface** values indicate −40°C ≤ T_J ≤ +125°C.

Parameter(s)	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Voltage						
V_{IN} range	VIN	**4.5**	—	**16**	V	
V_{IN} supply current	I_Q	—	2.5	—	mA	No switching, V_{FB} > +0.8V
Under Voltage Lockout (UVLO)						
V_{IN} UVLO upper threshold	VINUV_R	—	3.5		V	V_{IN} rising
V_{IN} UVLO hysteresis	VINUV_HYS	—	600	—	mV	
Output Voltage						
V_{OUT} Range	V_{OUT}	**0.6**	—	**3.46**	V	
VOUT voltage tolerance	VOUT_SET	–1.0	—	1.0	%V_{OUT}	V_{IN} = 12V, V_{OUT} = 1.2V
VOUT voltage tolerance	VOUT_SET	**–1.6**	—	**1.0**	%V_{OUT}	V_{IN} = 12V, V_{OUT} = 1.2V
Line regulation(2)	VOUT_DC_LINE	—	±0.1	—	%V_{OUT}	V_{IN} from 10.8V to 13.2V, I_{OUT} = 35A
Load regulation(2)	VOUT_DC_LOAD	—	±0.2	—	%V_{OUT}	I_{OUT} from 0A to 35A
V_{OUT} ripple(2)	VOUT_RIPPLE	—	20	—	mV_{P-P}	20 MHz bandwidth
Output Current						
I_{OUT} range(2)	I_{OUT}	**0**	—	**35**	A	Continuous
Protection						
Overcurrent(2)	OCP	—	130	—	%$I_{OUT(MAX)}$	
Overvoltage threshold(2)	OVP_{THRESH}	—	0.6	—	V	
Overvoltage hysteresis(2)	OVP_{HYST}	—	20	—	mV	

DC/AC Characteristics (continued)						
V_{IN} = 12V; V_{OUT} = 1.0V; f_{SW} = 400 kHz; T_A = +25°C, unless noted. **Boldface** values indicate −40°C ≤ T_J ≤ +125°C.						
Parameter(s)	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Thermal shutdown(1)	TSD	—	150	—	°C	Temperature rising
Thermal shutdown hysteresis(1)	THYST		15		°C	
PWM Controller						
EN threshold voltage	V_{EN_TH}		1.2		V	EN rising, point at which the output is enabled
EN threshold hysteresis	V_{EN_HYST}		50		mV	
Soft start	t_{SOFT_START}	—	2	—	ms	R_{SS} = Floating
PGOOD	VPG_TH		92		%VOUT	V_{FB} rising
	VPG_HYS	—	2	—	%VOUT	V_{FB} falling
	tD_PG	—	200	—	µs	V_{FB} rising, delay from FB high to PG high
	VPG_L	—	12	**200**	mV	VFB < 90% x VNOM, I_{PG} = 1 mA
Switching Frequency	f_{SW}	—	400	—	kHz	R_{FREQ} = 249 kΩ
Minimum On-Time(1)	TONMIN	—	40	—	ns	CCM
Minimum Off-Time(1)	TOFFMIN	—	100	—	ns	CCM
Performance						
Efficiency(2)	η	—	87	—	%	I_{OUT} = 35A
Transient response(2)	ΔV_{OUT_TRANS}	—	60	—	mV	10 A/µs load step from 25% to 75% of $I_{OUT(MAX)}$

Notes:

1. Ensured by design and characterization. Not production tested.
2. Not guaranteed; tested and characterized on EVB in defined application.

3.4. Thermal Characteristics

Parameter(s)	Symbol	Min.	Typ.	Max.	Unit	Conditions
Temperature Ranges						
Operating Junction Temperature Range(1)	T_J	−40	—	+125	°C	
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Temperature	T_S	−65	—	+150	°C	
Lead Temperature	T_{LEAD}	—	—	+300	°C	Soldering, 10s
Package Thermal Resistance						
Thermal Resistance, 11 × 17 mm LGA(2)	θ_{JA}	—	14.4	—	°C/W	

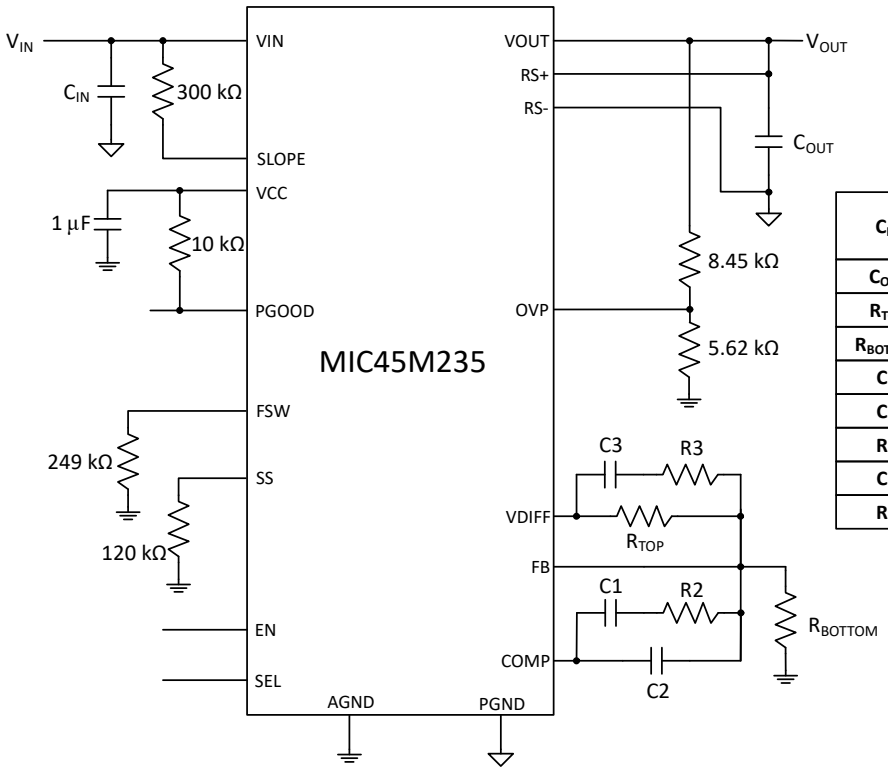
Notes:

1. The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.
2. Not guaranteed; based on thermal simulations. Case temperature refers to the hottest device within the MIC45M235, the powerstage.

4. Typical Performance Curves

Unless otherwise specified, the typical performance curves in this section were captured in the following configuration: V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 400 kHz, with Voltage Mode Control active, and using the configuration shown below.

Figure 4-1. Typical Performance Curves Configuration Schematic



C_{IN}	(16) 22 µF, 25V, X7R, 1210 (1) 220 µF, 25V, Al-Polymer
C_{OUT}	(16) 100 µF, 6.3V, X7S, 1210
R_{TOP}	34 kΩ
R_{BOTTOM}	49.9 kΩ
C1	2.7 nF
C2	68 pF
R2	10 kΩ
C3	390 pF
R3	1.4 kΩ

Figure 4-2. Efficiency vs. V_{IN}

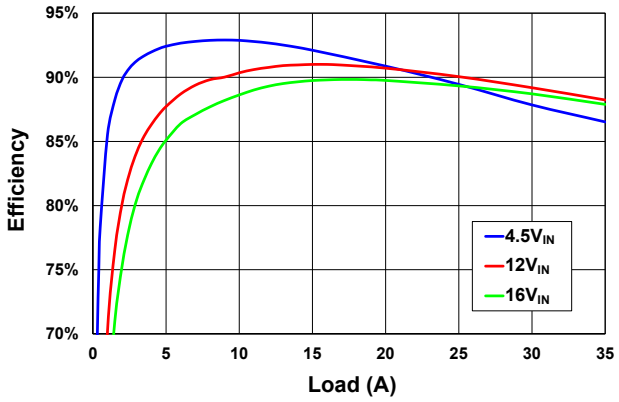


Figure 4-3. Power Loss vs. V_{IN}

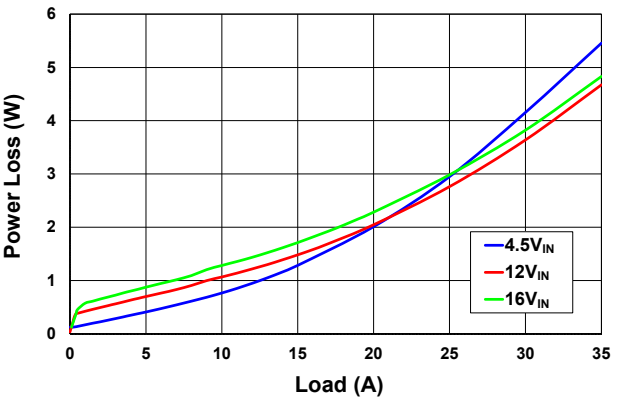


Figure 4-4. Efficiency vs. f_{SW}

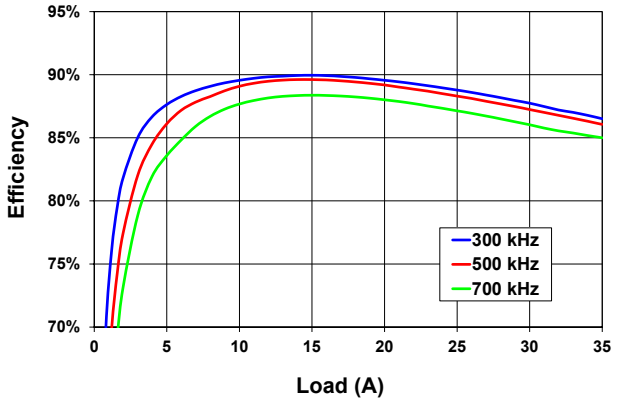


Figure 4-5. Power Loss vs. f_{SW}

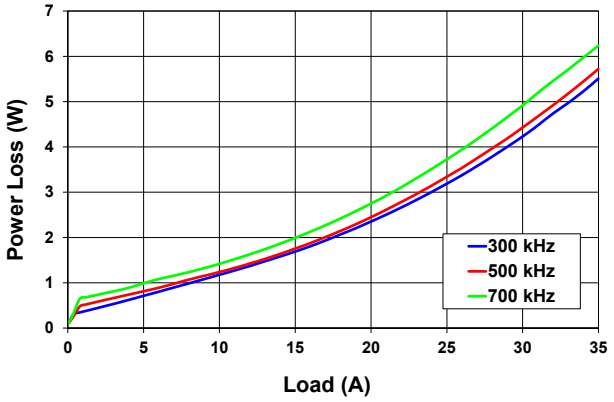


Figure 4-6. Efficiency vs. V_{OUT}

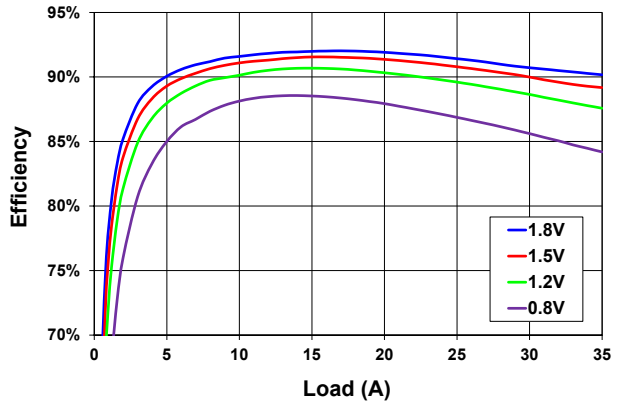


Figure 4-7. Power Loss vs. V_{OUT}

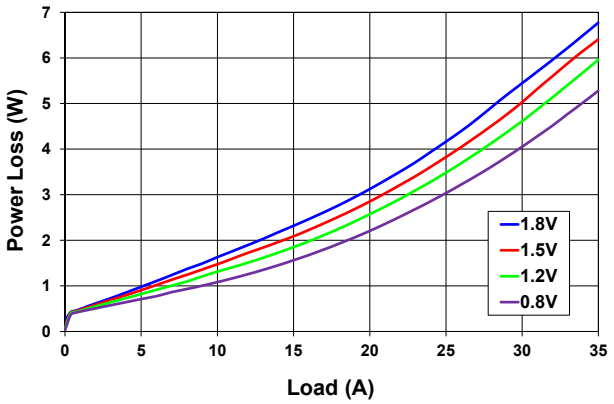


Figure 4-8. Load Regulation vs. V_{IN}

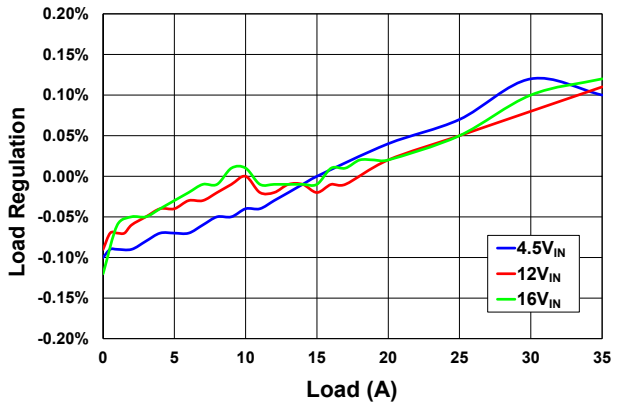


Figure 4-9. Load Regulation vs. Temperature

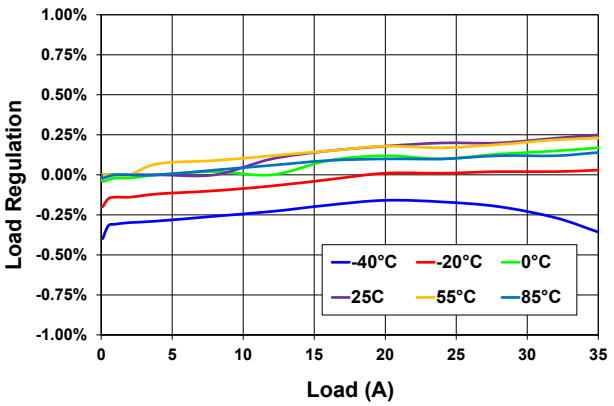


Figure 4-10. Startup (I_{OUT} = 20A, R_{SS} = 120 kΩ)

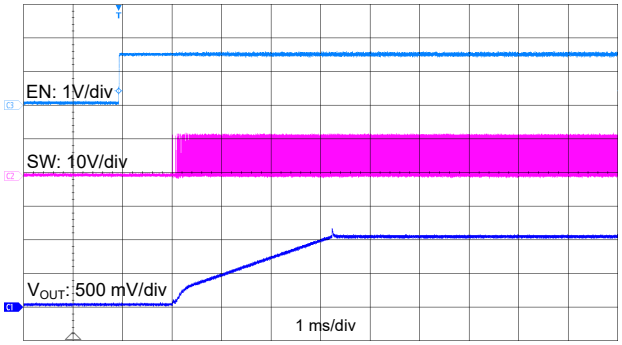


Figure 4-11. Startup (I_{OUT} = 24A, R_{SS} = 10 kΩ)

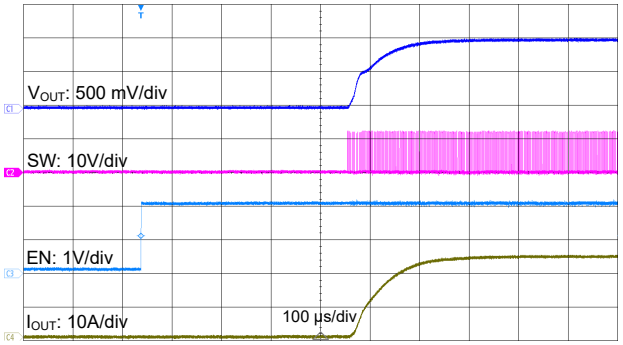


Figure 4-12. Switching Waveform

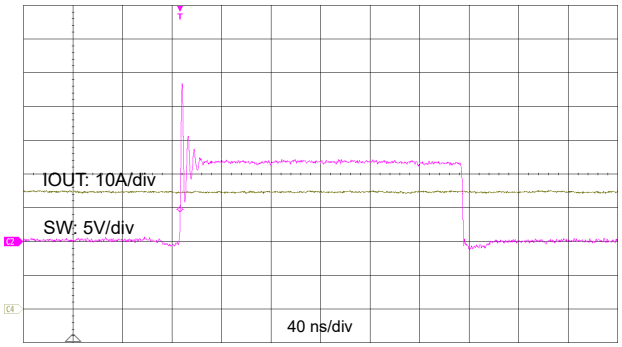


Figure 4-13. Load Transient (0.1A to 18A)

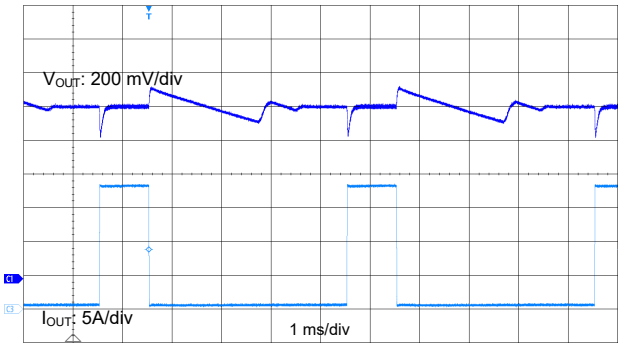


Figure 4-14. Load Transient (17A to 35A)

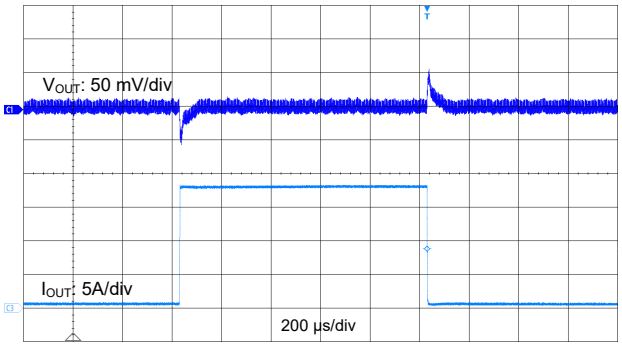


Figure 4-15. V_{OUT} Ripple

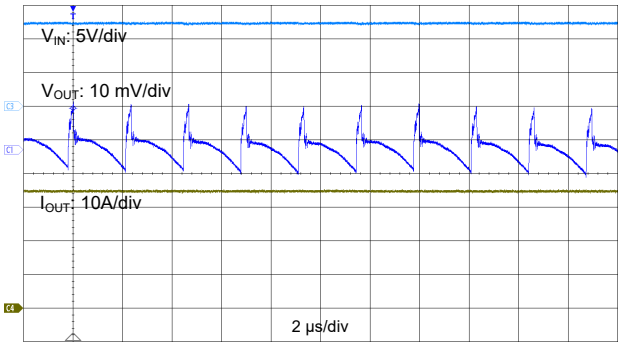


Figure 4-16. Current Limit Response

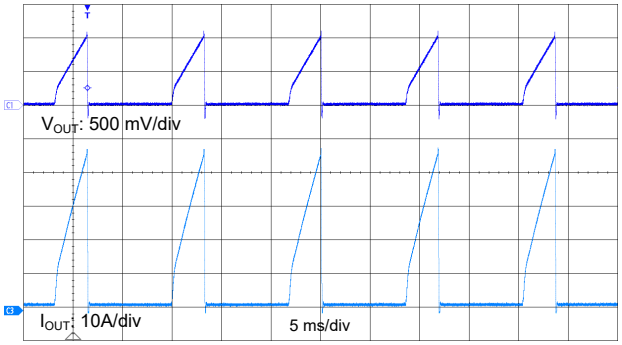


Figure 4-17. Current Limit vs. V_{IN}

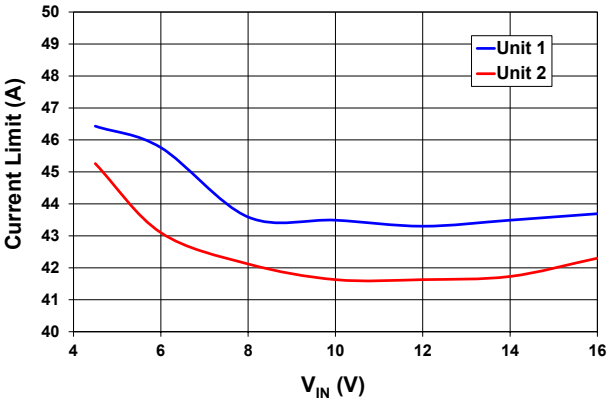


Figure 4-18. Current Limit vs. Temperature

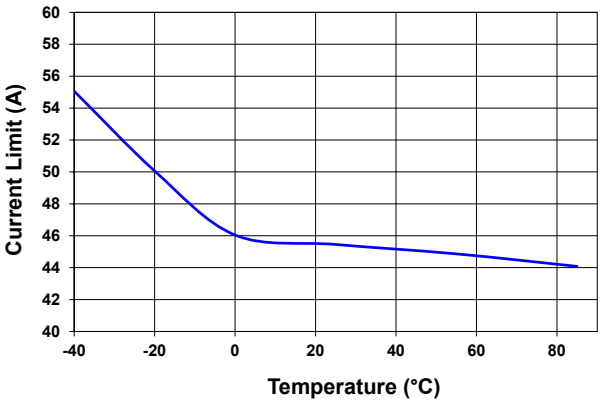
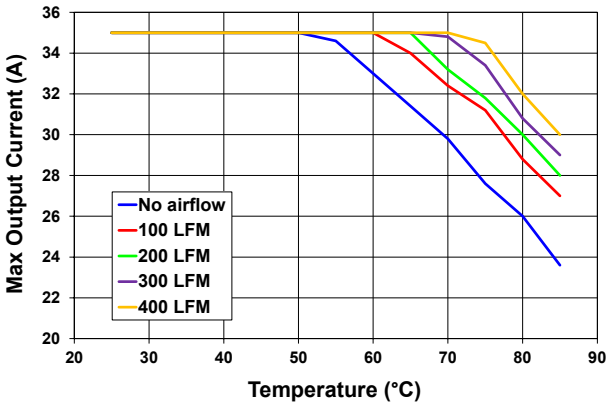


Figure 4-19. Current Derating vs. Temperature



5. Application Information

5.1. Input Capacitors

The input capacitors need to handle the peak and RMS input currents demanded by the MIC45M235. The capacitors also need to have low Equivalent Series Resistance (ESR) and inductance (ESL) to minimize input voltage ripple. Multi-Layer Ceramic Capacitors (MLCCs) are ideal for this purpose. In an 0805 case size, they can typically manage 2A RMS current with a temperature rise of less than 5°C, and a 1206 case size can typically support 3A RMS with minimal temp rise. The RMS value of the input current for the converter is estimated by using the formula:

Equation 5-1.

$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

Another important aspect of the input capacitors is to minimize input voltage ripple. Assuming the ESR of the ceramic capacitors is very low, ripple resulting from ESR can be ignored and Equation 5-2 can be used to estimate the required effective minimum input capacitance that will meet the ripple requirement.

Equation 5-2.

$$C_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{\text{eff} \cdot f_{SW} \cdot \Delta V_{INC}}$$

Where:

- D = Duty cycle
- eff = Converter efficiency
- ΔV_{INC} = Input Voltage peak-to-peak ripple

5.2. Output Capacitors

Two main requirements determine the size and characteristics of the output capacitor, C_{OUT}:

- Steady-state ripple
- Maximum voltage deviation during load transient

For steady-state ripple calculation, both the ESR and the capacitive ripple contribute to the total ripple amplitude. The MIC45M235 utilizes a low loss inductor, whose nominal value is 140 nH. From the switching frequency, input voltage, output voltage setting and load current, the peak-to-peak inductor current ripple can be calculated using Equation 5-3.

Equation 5-3.

$$\Delta L_{PP} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_{SW} \cdot 140\ \text{nH}}$$

With the inductor current ripple calculated, we can now estimate the minimum output capacitance required for a given voltage ripple specification using Equation 5-4.

Equation 5-4.

$$C_{OUT(MIN)} = \frac{\Delta L_{PP}}{8 \cdot f_{SW} \cdot \Delta V_{OUT\_PP\_C}}$$

Where:

- $\Delta V_{OUT\_PP\_C}$ = Capacitive component of Output Voltage Ripple, peak-to-peak

The output capacitor ESR will also contribute to the output ripple. Therefore, Equation 5-5 can be used to estimate the output voltage ripple.

Equation 5-5.

$$\Delta V_{OUT_{PP}} = \sqrt{\left(\frac{\Delta L_{PP}}{8 \cdot f_{SW} \cdot C_{OUT}}\right)^2 + (\Delta L_{PP} \cdot ESR_{COUT})^2}$$

The output capacitance must also be sized to handle load transients. When the load current changes from a lower value to a higher value (load step), the output voltage will temporarily decrease until the MIC45M235 is able to adjust the duty cycle to return the output voltage to its regulated value. This temporary output voltage decrease is known as output voltage undershoot. The converse happens when the load current changes from a higher value to a lower value (load dump), causing output voltage overshoot. The output capacitance must be sized to handle these transient conditions. There are various ways to estimate the minimum C_{OUT} required to maintain overshoot and undershoot, many of which do not account for the characteristics of the control loop. The following equation (5-6) is a decent estimate for the output voltage excursion due to load transients when accounting for the control loop bandwidth:

Equation 5-6.

$$\Delta V_{OUT\_TRAN} = \frac{\Delta I_{OUT\_TRAN}}{2\pi \cdot f_C \cdot C_{OUT}}$$

Where:

- ΔV_{OUT_TRAN} = Output Voltage excursion due to Load Transient
- ΔI_{OUT_TRAN} = Load Transient step
- f_C = Crossover frequency

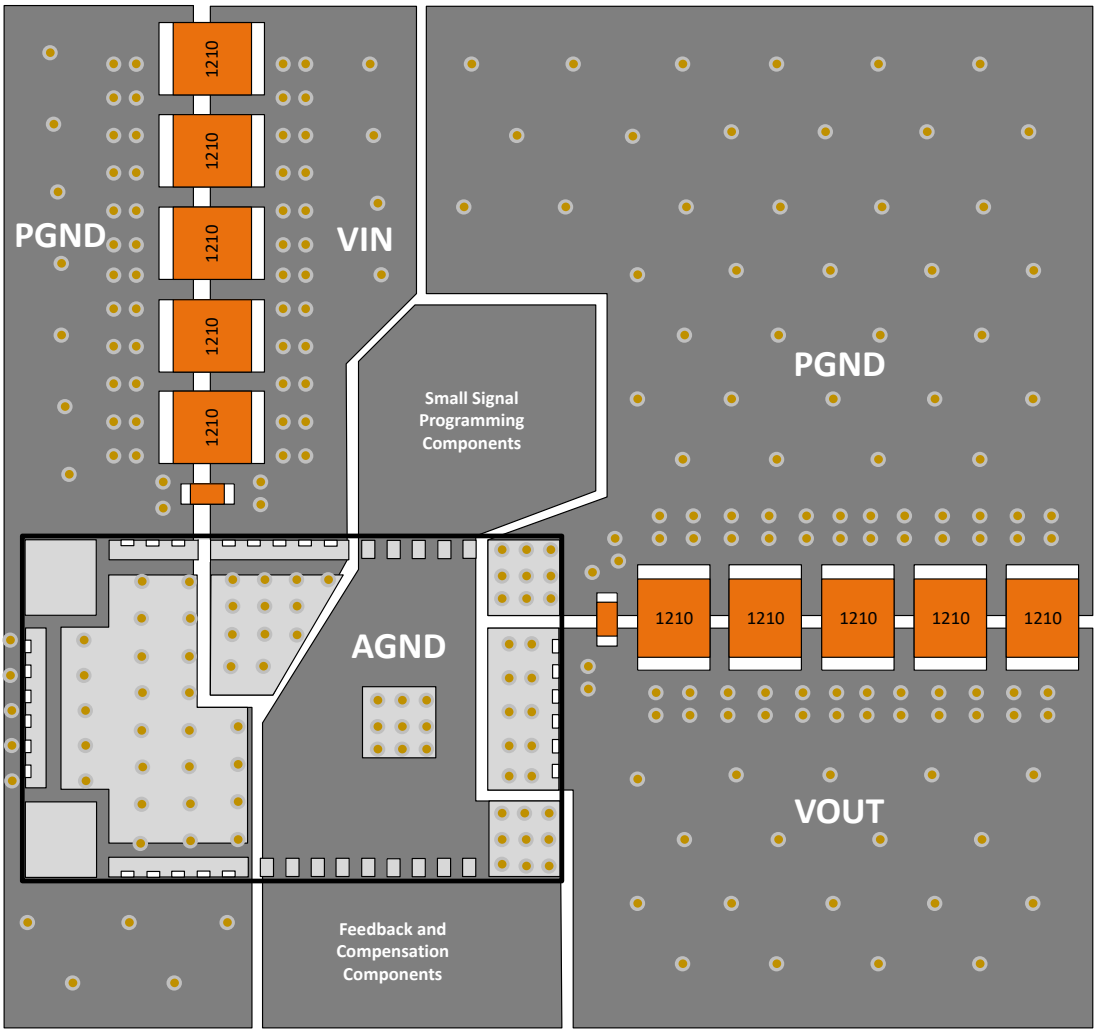
5.3. Layout Considerations

The high integration of MIC45M235 simplifies the PCB board layout. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Place bypass capacitors, including input/output capacitors, as close as possible to the MIC45M235's pins.
- Sense the output voltage with separate traces directly across the output capacitor bank. Route the differential feedback signals, RS+ and RS−, should be routed close together or on adjacent layers to minimize noise pickup.
- For thermal dissipation, connect the PGND pad to the power ground plane using vias. Copperfilled vias are preferred, but plated-through-hole vias are acceptable if not covered with solder mask.
- Use an adequate number of vias to connect between layers, especially for power traces.
- Connect AGND pins to the PGND copper layer using vias.
- To minimize power losses and improve thermal dissipation, use wide copper polygons for high current paths, including VIN, VOUT, and PGND.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce Module thermal stress, use multiple vias for interconnection between top layer and other power layers.

Figure 5-1 shows a good example of the top layer of the PCB, highlighting many of the bulleted points above.

Figure 5-1. Example PCB Top Layer



5.4. Module Reflow Profile Information

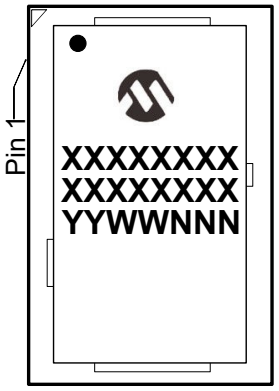
The MIC45M235 Module was assembled using the IPC/JEDEC J-STD-020 standard lead-free reflow profile and it can be soldered to the host board using standard leaded or lead-free solder reflow profiles. To avoid damaging the module, adhere to the following recommendations:

- For solder reflow recommendations, refer to the AN233 Solder Reflow Recommendation Application Note (DS00233).
- Do not exceed a peak temperature (TP) of 250°C.
- For specific reflow profile recommendations from the vendor, refer to the Solder Paste Data Sheet.
- Use only one flow. If the PCB requires multiple flows, apply the module on the final flow.

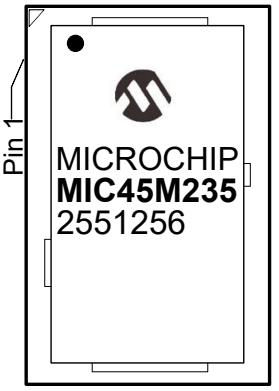
6. Packaging Information

Package Marking Information

44-Pin LGA (6.46 mm):



Example:



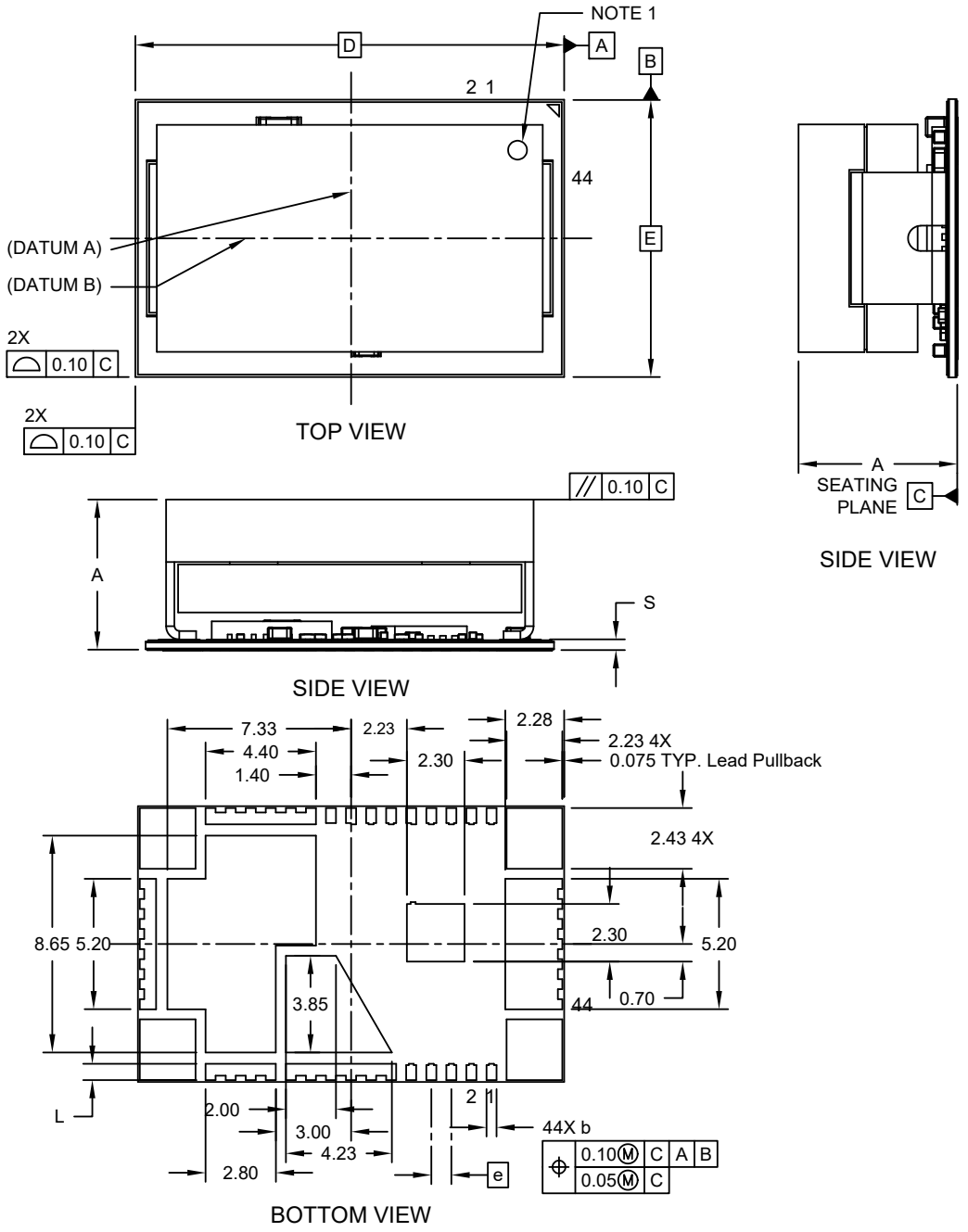
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

Package Outline Drawings

44-Lead Module (5JW) - 17x11x 6.46 mm Body [MODULE] With Multiple Ground Pads

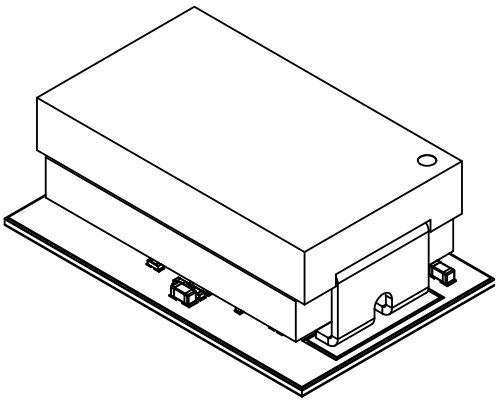
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-608 Rev A Sheet 1 of 2

44-Lead Module (5JW) - 17x11x 6.46 mm Body [MODULE] With Multiple Ground Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		44	
Pitch	e		0.80 BSC	
Overall Height	A	6.26	6.46	6.66
Substrate	S	0.42	0.50	0.56
Overall Length	D		17.00 BSC	
Overall Width	E		11.00 BSC	
Terminal Width	b	0.35	0.40	0.45
Terminal Length	L	0.55	0.60	0.65

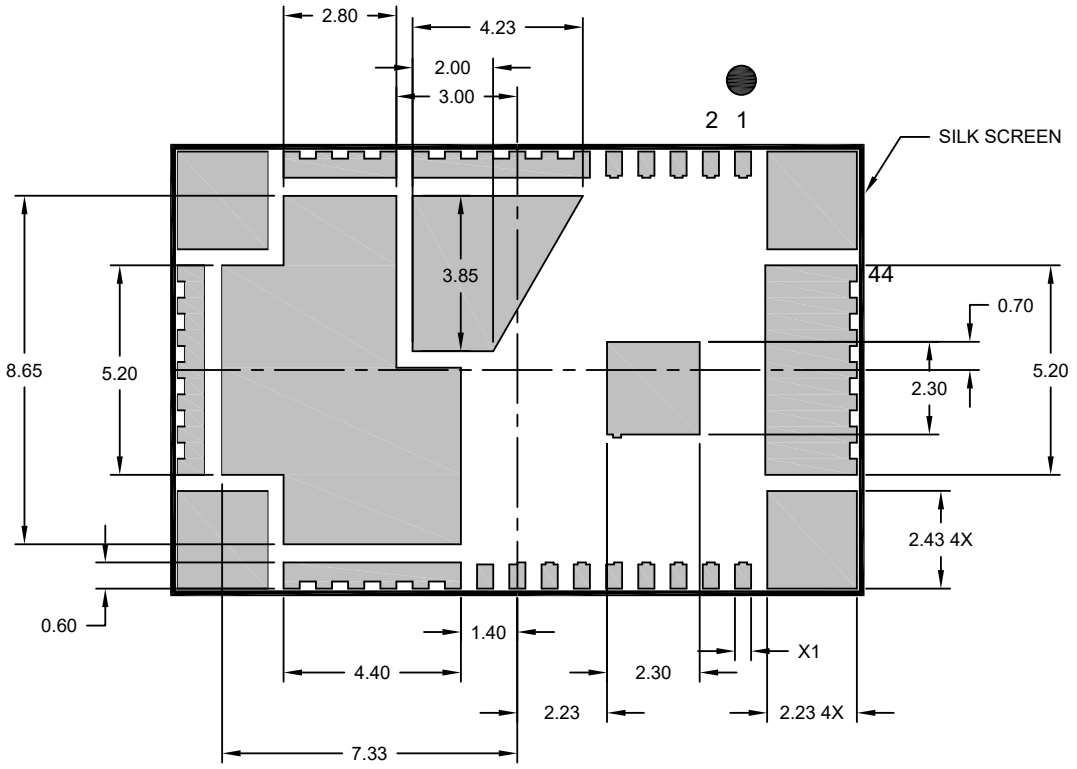
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
3. BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-608 Rev A Sheet 2 of 2

44-Lead Module (5JW) - 17x11x 6.46 mm Body [MODULE] With Multipule Ground Pads

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Notes:

1. All dimensions are in millimeters.

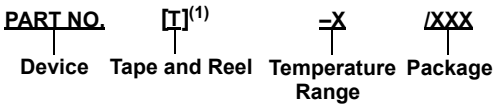
Microchip Technology Drawing C04-2608 Rev A

7. Revision History

Doc. Rev.	Date	Section	Comments
A	March 2026		Initial release of this document.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.



Device:	MIC45M235: 16V, 35A Switching Buck Regulator Module	
Tape & Reel Option(1):	Blank	= Tube
	T	= Tape and Reel
Temperature Range:	E	= −40°C to +125°C (Extended)
Package:	5JW	= Compact Module Land Grid Array (LGA), 44-Pin, 11 × 17 × 6.46 mm Package

Examples:

- MIC45M235-E/5JW: 16V, 35A Switching Buck Regulator Module, Tube, Extended Temperature Range, LGA 44-Pin Package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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