MC74HC175A

Quad D Flip-Flop with Common Clock and Reset

High−Performance Silicon−Gate CMOS

The MC74HC175A is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of four D flip−flops with common Reset and Clock inputs, and separate D inputs. Reset (active−low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive going edge of the Clock input.

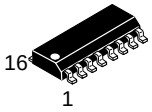
Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity 166 FETs or 41.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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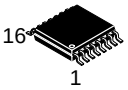
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MARKING DIAGRAMS

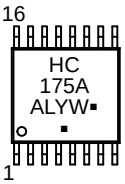


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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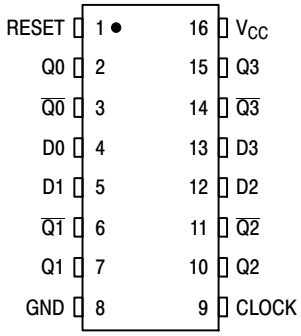


Figure 1. Pin Assignment

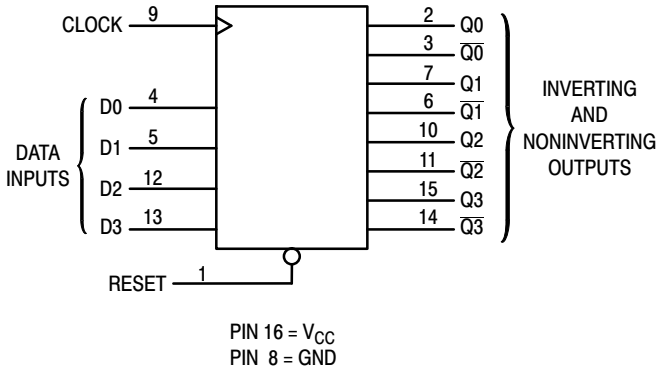


Figure 2. Logic Diagram

FUNCTION TABLE

Inputs			Outputs	
Reset	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	No Change	

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC175ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC175ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
MC74HC175ADTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
NLV74HC175ADTR2G*	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4 2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6 10 30 35	4.8 8.0 24 28	4 6 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0 3.0 4.5 6.0	150 75 26 22	190 90 32 28	225 110 38 33	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0 3.0 4.5 6.0	125 70 22 19	155 85 27 24	190 110 34 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Flip−Flop)*	35	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 3.0 4.5 6.0	100 45 20 17	125 65 25 21	150 85 30 26	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 3.0 4.5 6.0	5 3 3 3	5 3 3 3	5 3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	100 45 20 17	125 65 25 21	150 85 30 26	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	80 45 16 14	100 65 20 17	120 85 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	80 45 16 14	100 65 20 17	120 85 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

SWITCHING WAVEFORMS

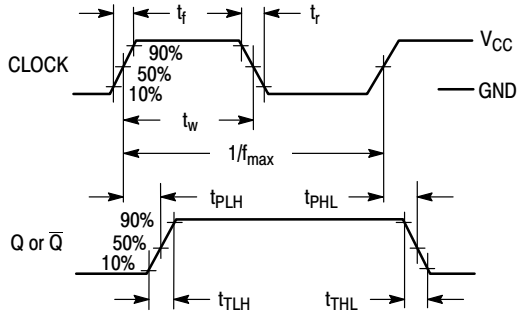


Figure 3.

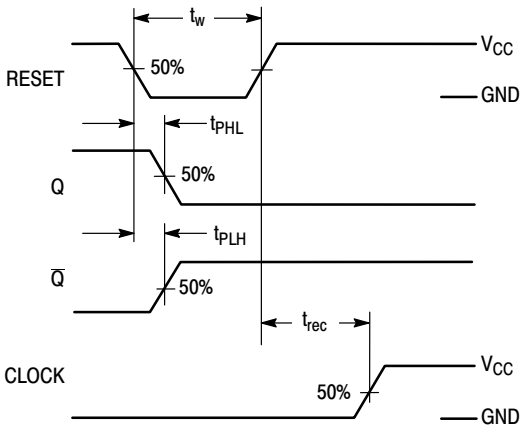


Figure 4.

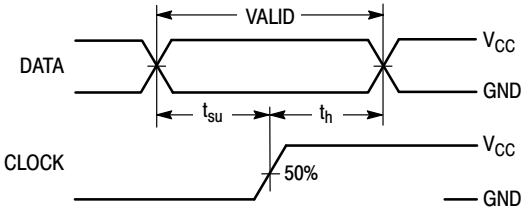
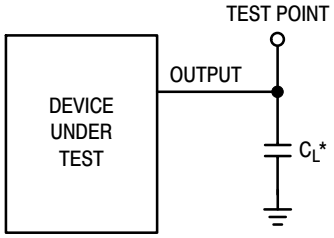


Figure 5.

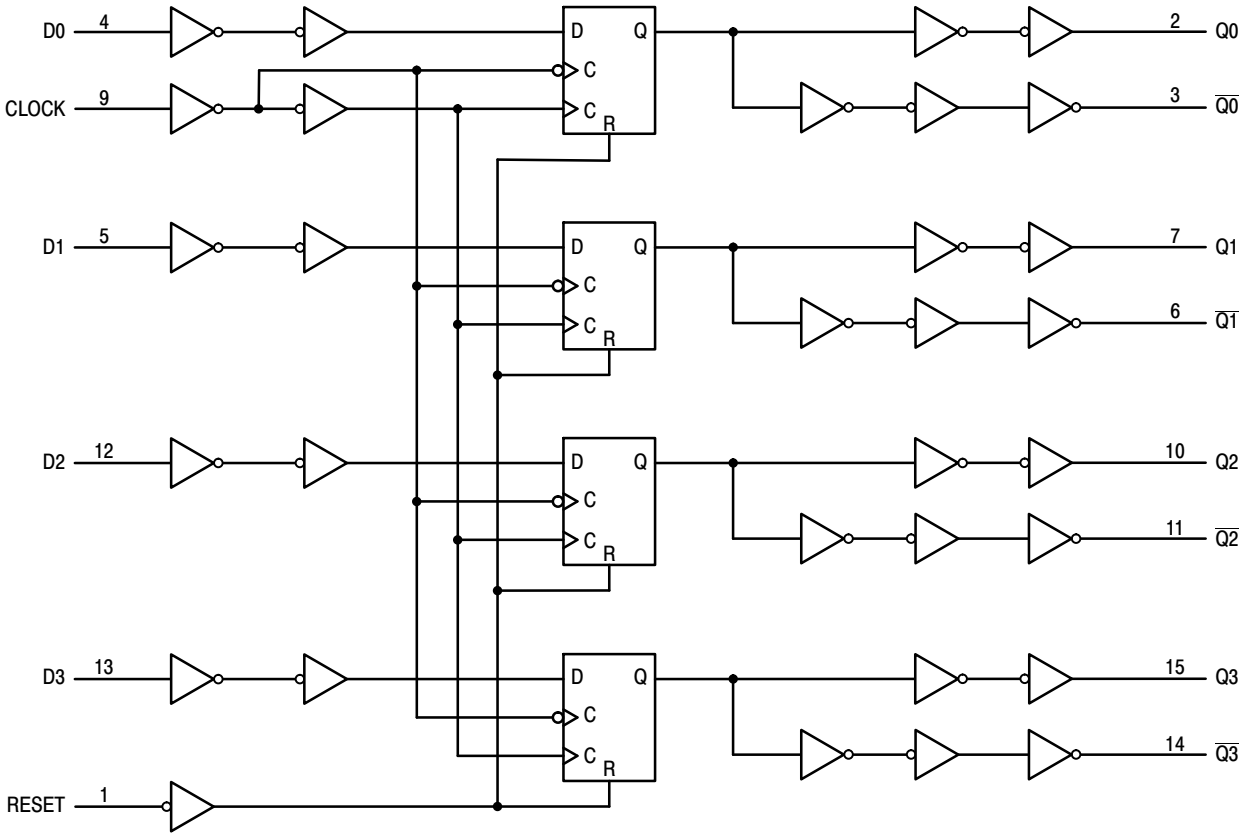
TEST CIRCUIT

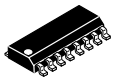


*Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM

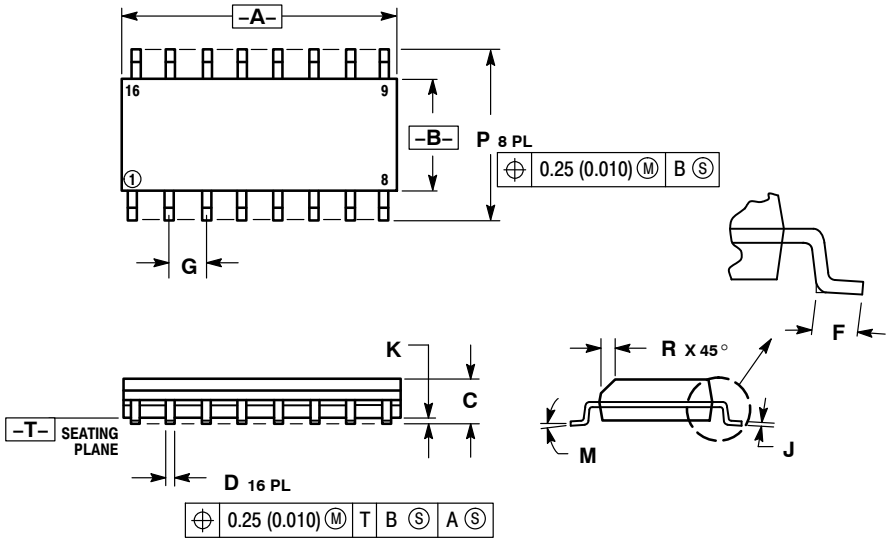




SCALE 1:1

SOIC–16
CASE 751B–05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

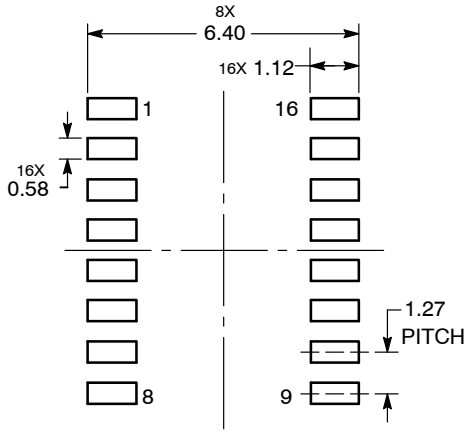
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

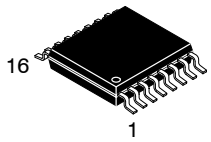
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

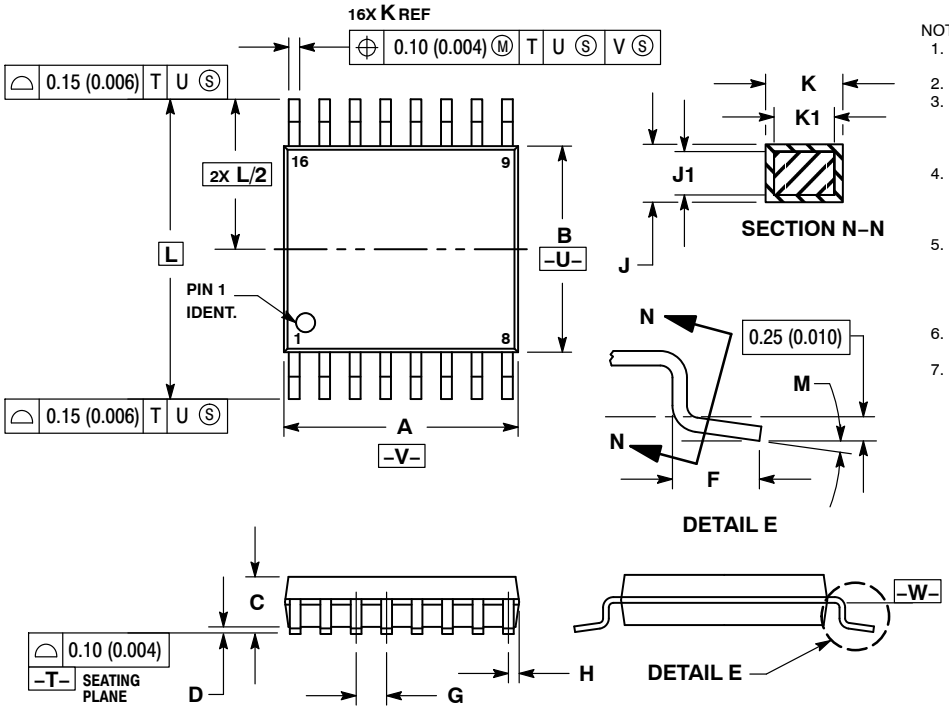
ON Semiconductor®



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

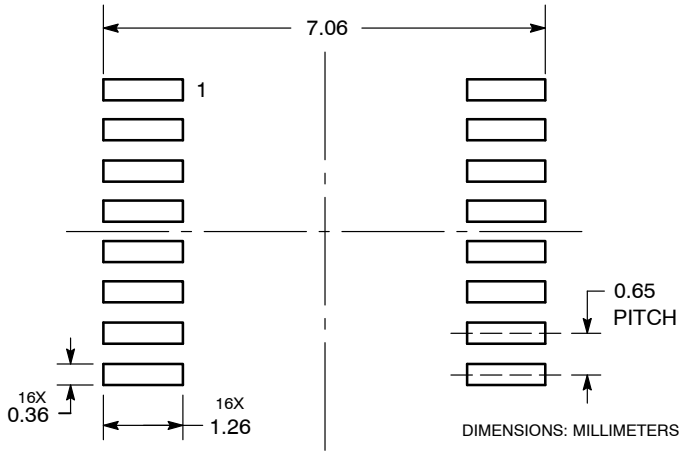
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

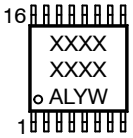
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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