

Description

The MCP1781 is a high-voltage, Low Drop-Out (LDO) regulator, capable of supplying 200 mA of output current. The input voltage range of 4.3V to 55V makes it suitable for 12V to 48V power rails, such as those found in high-voltage battery packs, or automotive applications where it can maintain regulation through large transients, including load dump events.

A low UVLO at shutdown of 2.3V makes it adequate for cold cranking conditions in automotive applications.

The MCP1781 comes in two standard fixed output voltage versions: 3.3V and 5.0V. The regulator output is stable with a 3.3 μ F ceramic capacitor. The device is protected from short-circuit events by the current foldback function and from overheating by means of thermal shutdown protection.

Two 5-lead packages are available, SOT-223 and TO-252, both with a PWG pin and a $\overline{\text{SHDN}}$ pin. While in shutdown, the quiescent current drops to 3.5 μ A, allowing for lower overall power consumption. The device itself has a ground current of 85 μ A typical, while delivering maximum output current of 200 mA.

Features

- AEC-Q100 Automotive Qualified (Grade 0, PPAP Capable)
- Wide Input Voltage Range: 4.3V to 55V
 - Undervoltage lock-out (UVLO): 2.7V typical
- Extended Junction Temperature Range: -40°C to $+150^{\circ}\text{C}$
- Standard Output Regulated Voltages (V_R): 3.3V and 5.0V ([Note](#))
 - Tolerance $\pm 2.0\%$ over temperature
- Open Drain Power Good Pin
- Low Quiescent Current: 34 μ A Typical
- Low Shutdown Current: 3.5 μ A Typical
- Output Current Capability: 200 mA Typical
- Short Circuit Current Foldback Protection
- Thermal Shutdown Protection: 169°C Typical
- Stable with Ceramic Output Capacitor: 3.3 μ F
- High PSRR for $V_{IN} = 14.5\text{V}$ and $I_{OUT} = 100\text{ mA}$:
 - -80 dB @ 100 Hz typical
 - -36 dB @ 100 kHz typical
- Available in the following Packages:
 - 5-Lead TO-252
 - 5-Lead SOT-223

Note: For other voltage options, contact your local sales office

1. Pin Configuration

1.1. Pin Descriptions

Table 1-1. Pin Descriptions Table

Pin Number (5-Pin SOT-223)	Pin Number (5-Pin TO-252)	Symbol	Description
1	1	SHDN	Shutdown Control Input. Do not leave this pin floating.
2	2	VIN	Input Voltage Supply
3	3	GND	Ground
4	4	VOU	Regulated Output Voltage
5	5	PWG	Open-drain Power Good; actively pulled low when VOU is below threshold.
6	6	Tab	Exposed Thermal Pad, connected to GND.

1.2. Package Types

Figure 1-1. 5-Lead SOT-223 Package.

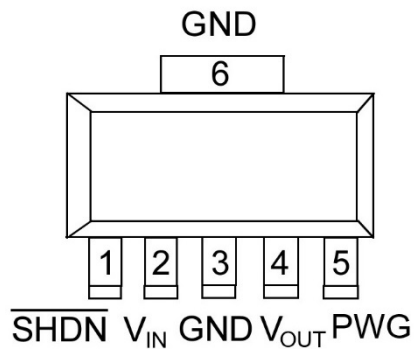
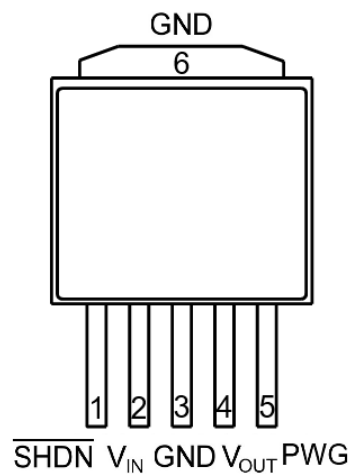


Figure 1-2. 5-Lead TO-252 Package.



1.3. Pin Details

1.3.1. Ground Pin (GND)

For optimal noise and Power Supply Rejection Ratio (PSRR) performance, the GND pin of the LDO should be tied to an electrically “quiet” circuit ground. This will ensure the LDO power supply rejection ratio and noise device performance. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower the inductance and, as a result, reduce the effect of fast current transients.

1.3.2. Regulated Output Voltage Pin (VOUT)

The VOUT pin is the regulated output voltage V_R of the LDO. A minimum output capacitance of 3.3 μF is required for the LDO to ensure the stability in all operating conditions. The MCP1781 is stable with ceramic capacitors. See [Section 2.2 “Output Capacitance Requirements”](#) for output capacitor selection guidance.

1.3.3. Input Voltage Supply Pin (VIN)

Connect the input voltage source to VIN. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 3.3 μF to 10 μF should be sufficient for most applications. The type of capacitor used is ceramic. The low ESR characteristics of the ceramic capacitor will yield better noise and PSRR performance at high frequency.

1.3.4. Shutdown Control Input ($\overline{\text{SHDN}}$)

The $\overline{\text{SHDN}}$ input is used to turn the LDO output voltage off. When the $\overline{\text{SHDN}}$ input is at a logic high level, the LDO output voltage is enabled. When the $\overline{\text{SHDN}}$ input is pulled to a logic low level, the LDO output voltage is disabled. When the $\overline{\text{SHDN}}$ input is pulled low, the LDO enters a low-quiescent current shutdown state, where the typical quiescent current is 3.5 μA .

1.3.5. Power Good Output (PWG)

PWG is an open drain output that can be connected to either 3.3V or 5V with a pull-up resistor, to monitor the status of the LDO regulated output voltage. When the regulated output voltage is above 94%, typically, the power good pin will indicate a logic high state. Similarly, if the value drops below 94% minus hysteresis, the pin will transition to a logic low state.

2. Functional Description

2.1. Device Overview

The MCP1781 is an AEC-Q100 qualified LDO capable of outputting 200 mA of current over its operating temperature range, while considering the acceptable power dissipation of the device. The part is stable with a minimum 3.3 μF ceramic capacitor and features a high-voltage SHDN pin, low voltage Power Good feedback for the regulated output voltage, current foldback protection and extended operating temperature range: -40°C to $+150^{\circ}\text{C}$. The device also features an adequate PSRR of -80 dB typical for low frequencies and -36 dB for high frequencies.

An innovative adaptive bias circuitry is used to lower the power consumption at no load and light loads, without compromising the dynamic response.

The internal discharge transistor is useful in powering microcontrollers and other applications that require fast supply disconnect.

2.2. Output Capacitance Requirements

The MCP1781 requires a minimum output capacitance of 3.3 μF for output voltage stability. The output capacitor should be located as close to the LDO output as possible. The device is designed to work with low ESR ceramic capacitors. Ceramic materials X8R/L or X7R have low temperature coefficients and are well within the acceptable ESR range required. A typical 3.3 μF X8R 0805 capacitor has an ESR of 50 m Ω . A higher output capacitance can help with better transient response.

2.3. Input Capacitance Requirements

Low input-source impedance is necessary for the LDO output to operate properly. When operating using battery power, or in applications with long lead length (> 10 inches) between the input source and the LDO, adding input capacitance is recommended. A minimum of 3.3 μF to 10 μF of capacitance is sufficient for most applications. Given the high input voltage capability of the MCP1781, of up to 55V DC, it is recommended to use an appropriate voltage rating capacitor, and the derating of the capacitance as a function of voltage and temperature needs to be considered. The ceramic capacitor type should be X7R or X8R/L because their dielectrics are rated for use with temperatures between -40°C to $+125^{\circ}\text{C}$ or -55°C to $+150^{\circ}\text{C}$, respectively.

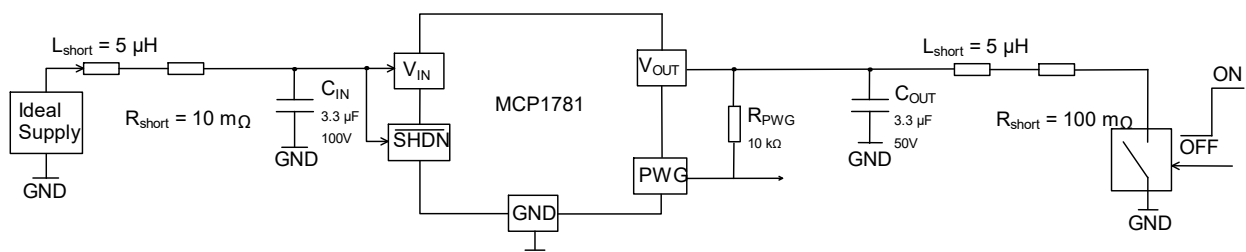
2.4. Circuit Protection

The MCP1781 features current foldback protection during an output short-circuit event that occurs during normal operation. When the current foldback block detects an increase in load current, over the typical value of 450 mA, the output current and output voltage will start to decrease until the output current reaches a value of typically 10 mA (see [Figure 4-16](#) and [Figure 4-17](#)).

If a short circuit is present during power-up, the part will enter in current limit protection and a constant current of 450 mA will be maintained. The part will not enter in current foldback.

The MCP1781 was tested using the AEC-Q100 test set-up in [Figure 2-1](#). The testing conditions require the use of very high parasitic inductances on the input and output. For cases like this, it is required to prevent the output voltage going below ground with more than 1V. Note that the VOUT pin can withstand a maximum of -0.3 VDC (see [Absolute Maximum Ratings](#)). This can be achieved by placing a diode with the cathode to VOUT and the anode to ground.

Thermal shutdown functionality is present on the device and adds to the protection features of the part. Thermal shutdown is triggered at a typical value of 169°C and has a typical hysteresis of 11°C .

Figure 2-1. Short Circuit Test Setup.

2.5. Dropout Operation

In automotive applications, depending on the severity of the cold crank, the supply voltage can drop down to 3V and the part can enter dropout in these conditions. It is preferred to ensure that the part does not operate in dropout during DC operation so that the AC performance is maintained.

The device has a dropout voltage of approximately 380 mV at full load and room temperature, but because of the extended temperature range at 150°C, due to increased leakage, it reaches up to 705 mV.

2.6. Shutdown Input ($\overline{\text{SHDN}}$) and Input UVLO

The $\overline{\text{SHDN}}$ input is an active-low input signal that turns the LDO ON or OFF. The $\overline{\text{SHDN}}$ threshold has a logic HIGH level of minimum 1.13V and a logic LOW level of maximum 0.79V.

The $\overline{\text{SHDN}}$ pin ignores low-going pulses that are up to 10 μs . This blanking window helps to reject any system noise spikes on the $\overline{\text{SHDN}}$ input signal. Then, on the rising edge of the $\overline{\text{SHDN}}$ input, the shutdown circuitry adds 600 μs delay before allowing the regulator output to turn ON. This delay helps to reject any false turn-on signals or noise on the $\overline{\text{SHDN}}$ input signal. After the (10 + 600) μs delay, the regulator starts charging the load capacitor as the output rises from 0V to its regulated value. The charging current amplitude will be limited by the short circuit current value of the device. If the $\overline{\text{SHDN}}$ input signal is pulled low during the 610 μs delay period, the timer will be reset, and the delay time will start over again on the next rising edge of the $\overline{\text{SHDN}}$ input. Figure 2-2 shows a timing diagram of the $\overline{\text{SHDN}}$ input.

The MCP1781 has an internal discharge transistor connected to the VOUT Pin that is enabled when the $\overline{\text{SHDN}}$ pin goes low. The discharge occurs through a typical resistance of 105 Ω .

The UVLO block helps prevent false start-ups during the power-up sequence, until the input voltage reaches a value of 2.7V. The minimum input voltage required for normal operation needs to take into account the dropout voltage for the specific output voltage and output current conditions.

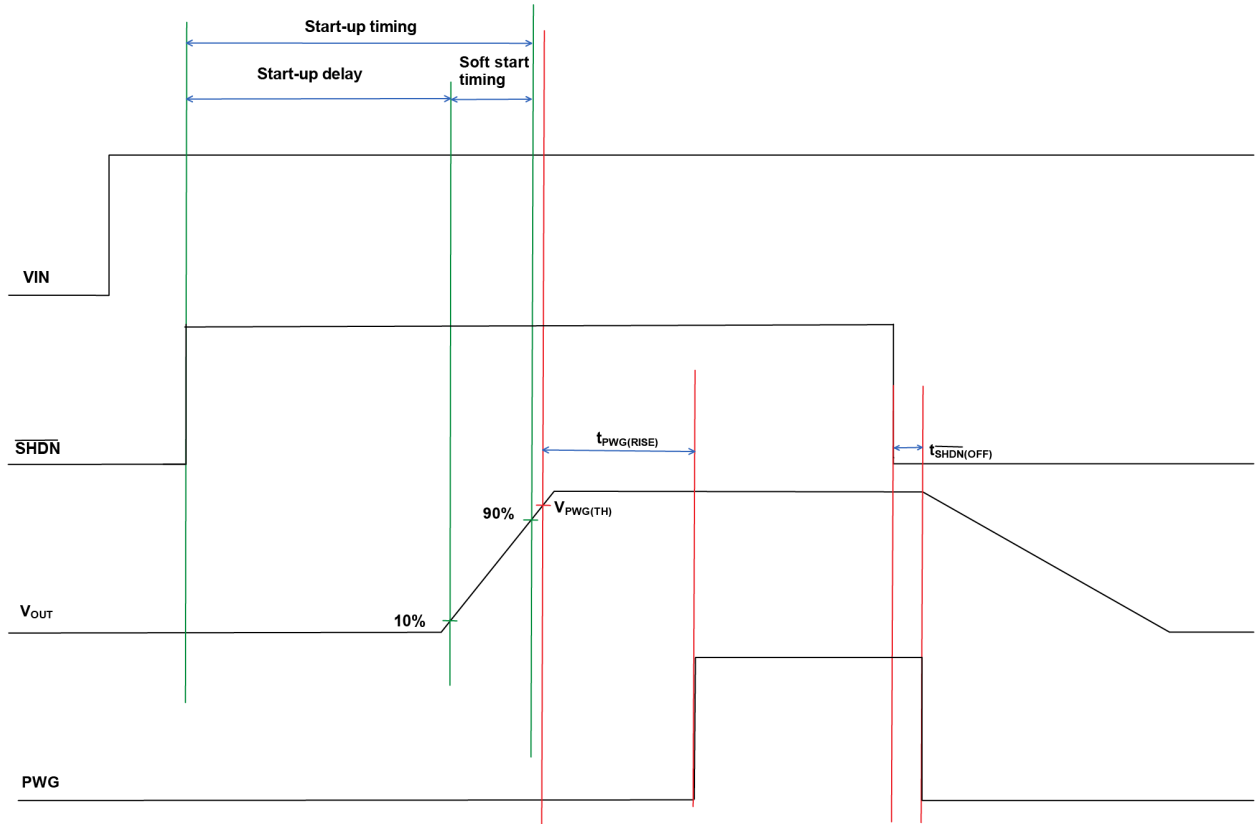
2.7. Power Good

The Power Good function is a low voltage open drain output which can be used to monitor the output of the LDO in relation with the Power Good Threshold level ($V_{\text{PWG(TH)}}$), which is typically 94% of the output voltage.

During a normal start up sequence the open drain output is held low until the monitored regulated output voltage reaches the value of $V_{\text{PWG(TH)}}$. After which the power good time delay ($t_{\text{PWG(RISE)}}$) will start, and after 98 μs typically the PWG pin will become inactive and can be pulled high by the external pull up resistor connected to VOUT or a separate supply rail that is below 5.5V.

During transient events, false triggering of the Power Good signal is prevented by means of time delay ($t_{\text{PWG(FALL)}}$), typically, of 105 μs . After the internal circuitry detects the regulated output falling below the $V_{\text{PWG(TH)}}$ minus $V_{\text{PWG(HYS)}}$, the open drain output won't be pulled low until the time delay passes. When the $\overline{\text{SHDN}}$ is pulled low, if the requirements for a valid signal are met, then the Power Good open drain will be pulled low. The output will be discharged by the output discharge block by means of 105 Ω resistor pulled down to GND.

Figure 2-2. Shutdown Input Timing Diagram



3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Input Voltage	+70.0V
Maximum Voltage on $\overline{\text{SHDN}}$	(GND - 0.3V) to ($V_{\text{IN}} + 0.3\text{V}$)
Maximum Voltage on VOUT	(GND - 0.3V) to 5.5V
Maximum Voltage on PWG	(GND - 0.3V) to 5.5V
Output Short-Circuit Duration	Unlimited (Note 2)
Storage Temperature	-55°C to +175°C
Maximum Junction Temperature, T_{J}	+185°C
Operating Junction Temperature, T_{J}	-40°C to +150°C
ESD Protection on All Pins:	
HBM	$\geq \pm 2$ kV
CDM	$\geq \pm 750\text{V}$



Attention: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2. DC/AC Characteristics

Electrical Specifications: Unless otherwise noted, $V_{\text{IN}} = V_{\text{R}} + 1\text{V}$ (Note 1), $I_{\text{OUT}} = 1$ mA, $C_{\text{IN}} = C_{\text{OUT}} = 3.3$ μF ceramic (X7R), $T_{\text{J}} = +25^\circ\text{C}$, $\overline{\text{SHDN}} > 2.4\text{V}$. **Boldface** type applies for ambient temperatures T_{J} of -40°C to $+150^\circ\text{C}$ (Note 2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
DC Performance						
Input Operating Voltage	V_{IN}	4.3	—	55	V	$V_{\text{OUT}} = 3.3\text{V}$
		6	—	55	V	$V_{\text{OUT}} = 5.0\text{V}$
Output Voltage Accuracy	V_{OUT}	$V_{\text{R}} - 2\%$	V_{R}	$V_{\text{R}} + 2\%$	%	—
Input Quiescent Current	I_{Q}	—	34	57	μA	$V_{\text{IN(MIN)}} \leq V_{\text{IN}} \leq 55\text{V}$; $I_{\text{OUT}} = 0$ mA
Input Quiescent Current for $\overline{\text{SHDN}}$ Mode	$I_{\overline{\text{SHDN}}}$	—	3.5	15	μA	$\overline{\text{SHDN}} = \text{GND}$, $V_{\text{IN}} = 55\text{V}$
Ground Current	I_{GND}	—	85	122	μA	$I_{\text{GND}} = I_{\text{IN}} - I_{\text{OUT}}$ $I_{\text{OUT}} = 200$ mA
Maximum Output Current	I_{OUT}	200	—	—	mA	(Note 2)
Line Regulation	$\Delta V_{\text{OUT}} / (V_{\text{OUT}} \times \Delta V_{\text{IN}})$	-0.005	± 0.002	+0.005	%/V	$V_{\text{IN(MIN)}} \leq V_{\text{IN}} \leq 55\text{V}$
Load Regulation	$\Delta V_{\text{OUT}} / V_{\text{OUT}}$	-0.1	± 0.06	+0.1	%	$I_{\text{OUT}} = 1$ mA to 200 mA
Dropout Voltage	V_{DROPOUT}	—	380	705	mV	$I_{\text{OUT}} = 200$ mA (Note 3)
AC Performance						
Output Noise	e_{N}	—	300	—	μVrms	$f = 10$ Hz to 10 MHz, $V_{\text{IN}} = 16\text{V}$, $I_{\text{OUT}} = 100$ mA (Note 5)

DC/AC Characteristics (continued)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Rejection Ratio	PSRR	—	-80	—	dB	f = 100 Hz (Note 4) (Note 5)
		—	-65	—		f = 1 kHz (Note 4) (Note 5)
		—	-36	—		f = 100 kHz (Note 4) (Note 5)
Current Limit						
Foldback Current Limit	I_{CL}	—	450	—	mA	(Note 5)
Foldback Current	$I_{FOLDBACK}$	—	10	—	mA	$V_{OUT} \approx 0V$ (Note 5)
Undervoltage Lock Out						
Input Voltage to Turn-on Output	$V_{UVLO(HI)}$	—	2.7	—	V	Rising V_{IN}
Input Voltage to Turn-off Output	$V_{UVLO(LO)}$	—	2.3	—	V	Falling V_{IN}
Shutdown						
Logic High Input	$V_{SHDN(HI)}$	1.13	—	—	V	
Logic Low Input	$V_{SHDN(LO)}$	—	—	0.79	V	
\overline{SHDN} Input Leakage Current	$I_{SHDN(LK)}$	—	—	0.22	μA	$V_{SHDN} = 55V$
Turn-off delay	$t_{SHDN(OFF)}$	—	22	—	μs	V_{SHDN} Falling (Note 5)
Soft Start						
Soft Start Timing	t_{SS}	—	450	720	μs	From 10% of V_R to 90% of V_R
Start-up Delay	t_{DELAY}	—	600	—	μs	From $V_{IN} = V_{SHDN} = 0V$ to $V_R + 1V$, until $V_{OUT} = 10\%$ of V_R (See Note 5)
Power Good						
Power Good Threshold	$V_{PWG(TH)}$	90	94	97	% V_{OUT}	Rising V_{OUT}
Power Good Hysteresis	$V_{PWG(HYS)}$	1	3	6	% V_{OUT}	Falling V_{OUT}
Power Good Sink Capability	$I_{PWG(SINK)}$	5	—	—	mA	
Power Good Output Voltage Low	$V_{PWG(VOL)}$	—	36	66	mV	$I_{PWG(SINK)} = 5 mA$; $V_{OUT} = 0V$
Power Good Leakage	$I_{PWG(LKG)}$	—	—	20	nA	$V_{PWG} = 5.5V$
Power Good Delay Rising	$t_{PWG(RISE)}$	—	98	—	μs	Delay after V_{OUT} crosses Power Good Threshold (Note 5)
Power Good Delay Falling	$t_{PWG(FALL)}$	—	105	—	μs	Delay after V_{OUT} crosses Power Good Threshold minus Hysteresis (Note 5)
Output Discharge Transistor						
Discharge Resistance	$R_{DS(ON)}$	—	105	—	Ω	(Note 5)

DC/AC Characteristics (continued)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Notes:						
1.	VR is the nominal output voltage. The minimum input voltage is 4.3V for $V_R = 3.3V$ and 6V for $V_R = 5V$.					
2.	The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). See the Temperature Specifications table and Section 5. Application Information . Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.					
3.	Dropout voltage is defined as the input to output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 1V$.					
4.	PSRR measurement is carried out with $C_{IN} = 0 \mu F$, $V_{IN} = 14.5V$, $I_{OUT} = 100 \text{ mA}$, $V_{INAC} = 0.4 V_{pkpk}$.					
5.	Not production tested.					

3.3. Temperature Specifications

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Thermal Shutdown	T_{SD}	—	169	—	°C	Rising Temperature (not production tested)
Thermal Shutdown Hysteresis	ΔT_{SD}	—	11	—	°C	Falling Temperature (not production tested)
Thermal Package Resistances						
Thermal Resistance, SOT-223-5LD	θ_{JA}	—	68.3	—	°C/W	JEDEC® standard 4-layer FR4 board with 1 oz. copper
	θ_{JB}	—	18.3	—	°C/W	
	Ψ_{JT}	—	6.6	—	°C/W	
Thermal Resistance, TO-252-5LD	θ_{JA}	—	32.7	—	°C/W	
	θ_{JB}	—	8.3	—	°C/W	
	Ψ_{JT}	—	3.8	—	°C/W	

4. Typical Performance Curves

➔ Important: The graphs provided in this section are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Figure 4-1. Output Voltage vs. Input Voltage (3.3V).

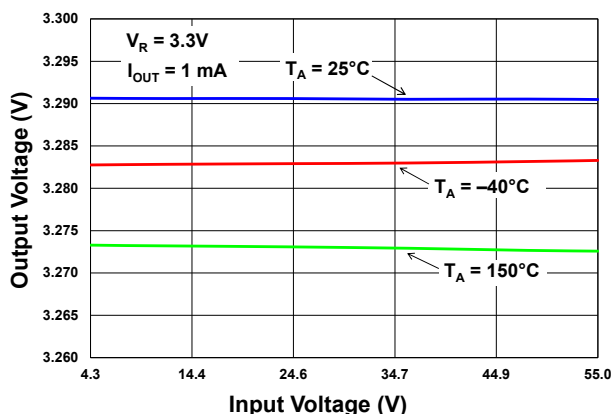


Figure 4-2. Output voltage vs. Input Voltage (5V).

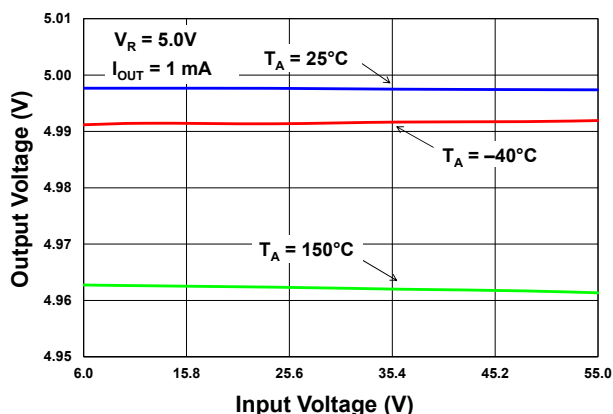


Figure 4-3. Output Voltage vs. Output Current (3.3V).

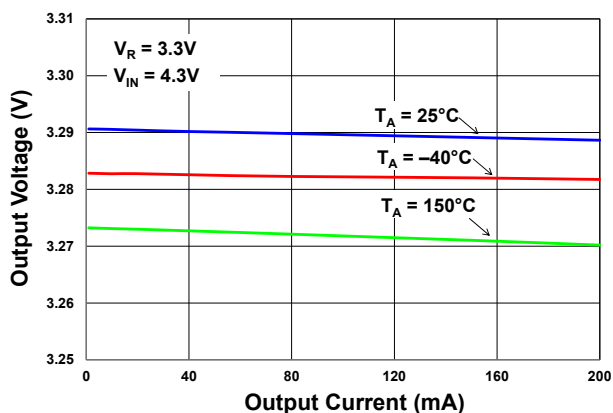


Figure 4-4. Output Voltage vs. Output Current (5V).

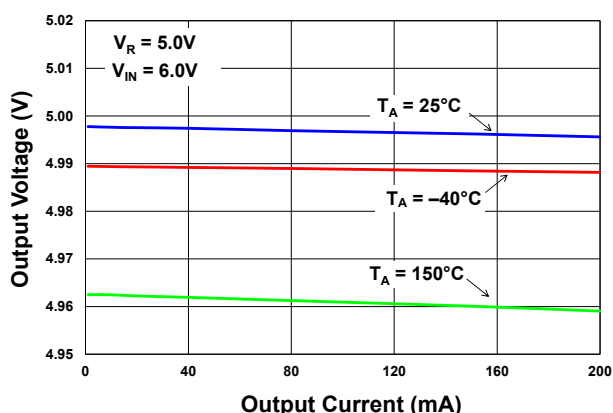


Figure 4-5. Dropout Voltage vs. Load Current (5V).

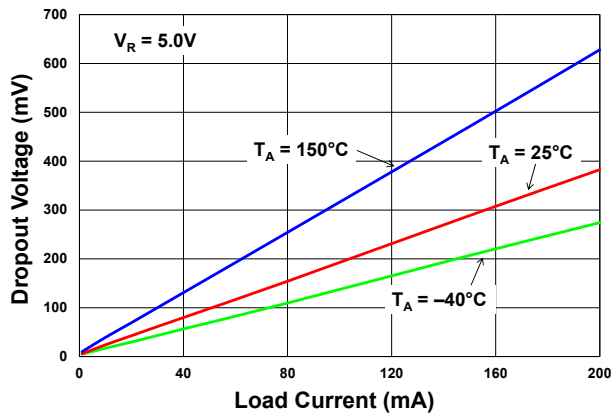


Figure 4-6. Load Regulation vs. Ambient Temperature (3.3V).

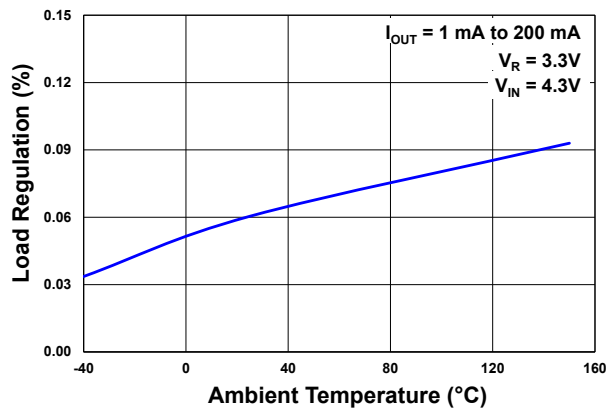


Figure 4-7. Load Regulation vs. Ambient Temperature (5V).

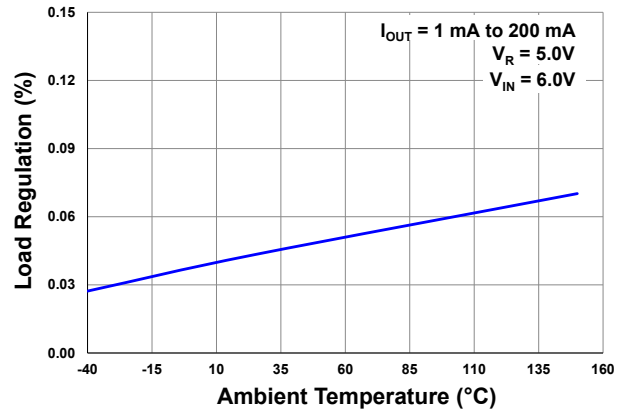


Figure 4-8. Line Regulation vs. Ambient Temperature (3.3V).

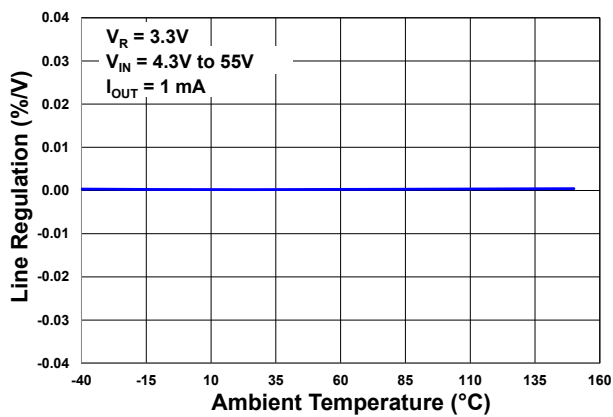


Figure 4-9. Line Regulation vs. Ambient Temperature (5V).

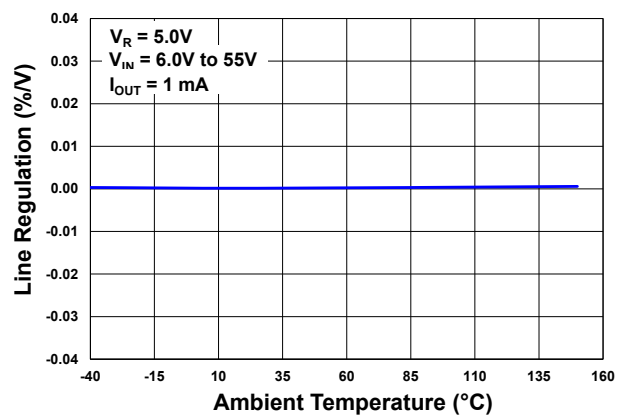


Figure 4-10. Quiescent Current vs. Input Voltage (3.3V).

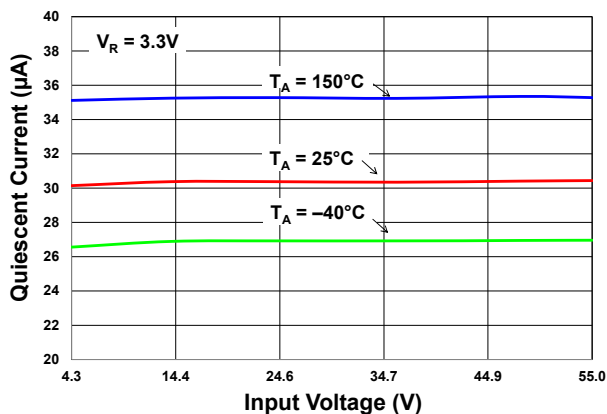


Figure 4-11. Quiescent Current vs. Input Voltage (5V).

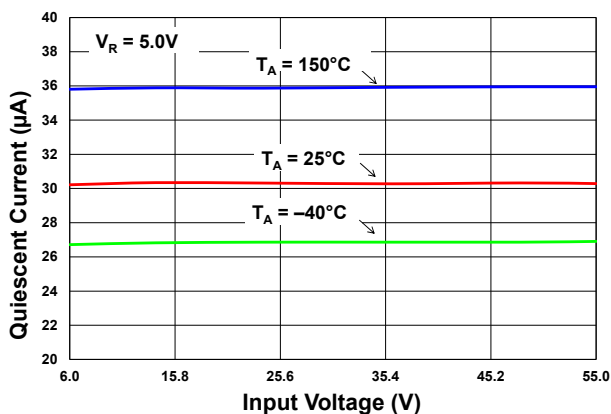


Figure 4-12. Shutdown Current vs. Input Voltage (3.3V).

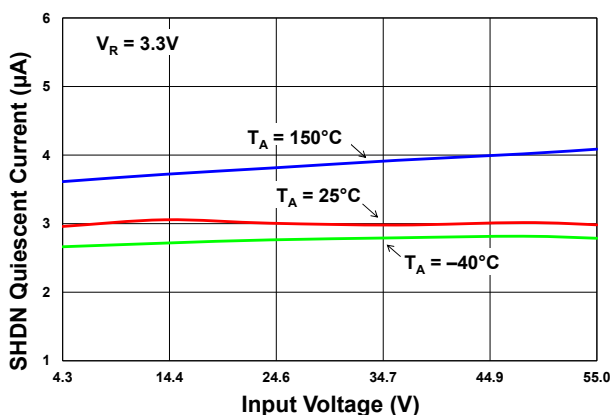


Figure 4-13. Shutdown Current vs. Input Voltage (5V).

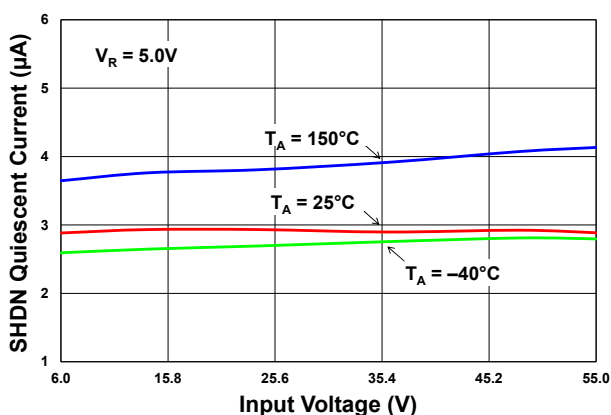


Figure 4-14. Ground Current vs. Output Current (3.3V).

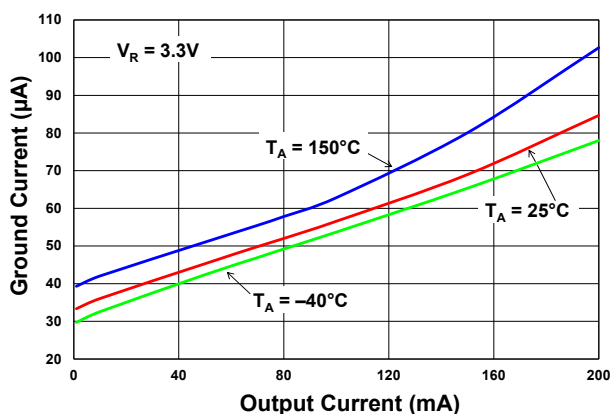


Figure 4-15. Ground Current vs. Output Current (5V).

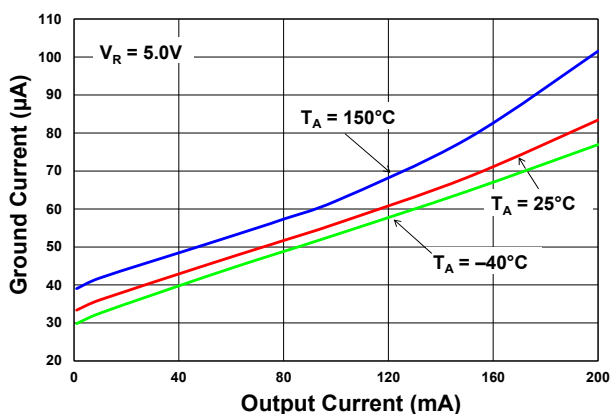


Figure 4-16. Current Foldback (3.3V).

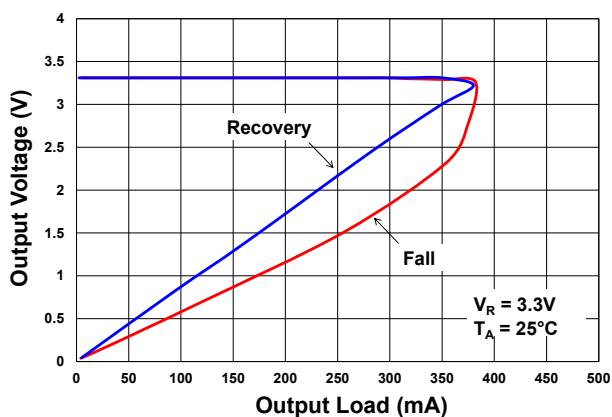


Figure 4-17. Current Foldback (5V).

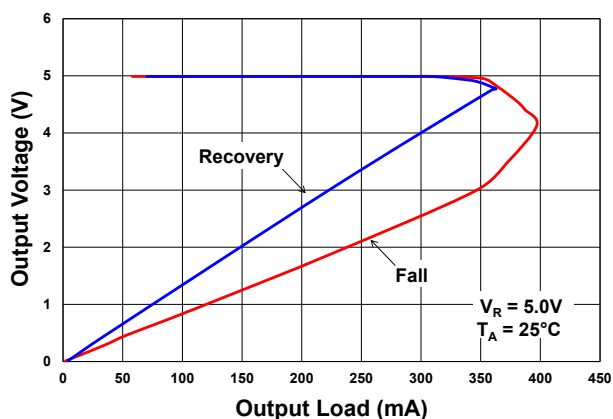


Figure 4-18. UVLO (3.3V).

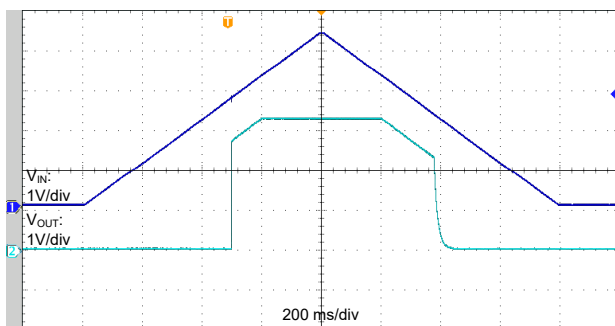


Figure 4-19. UVLO (5V).

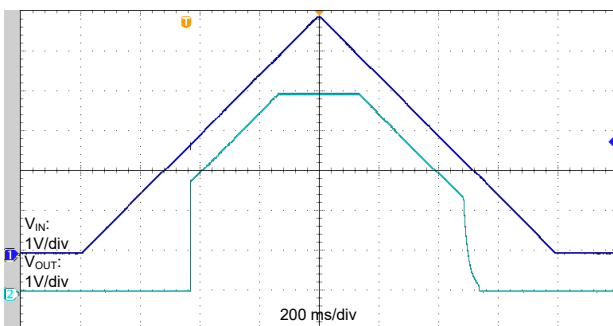


Figure 4-20. Noise vs. Frequency (3.3V).

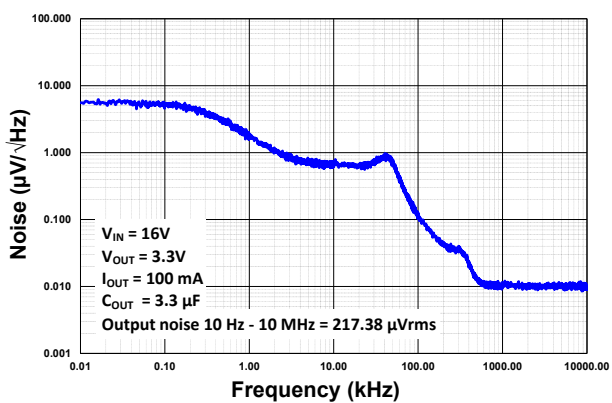


Figure 4-21. Noise vs. Frequency (5V).

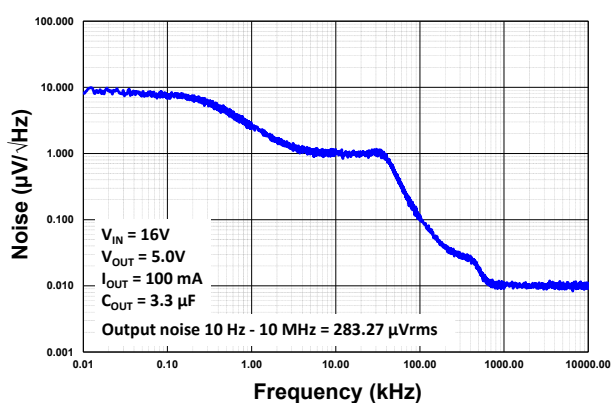


Figure 4-22. PSRR vs. Frequency (3.3V).

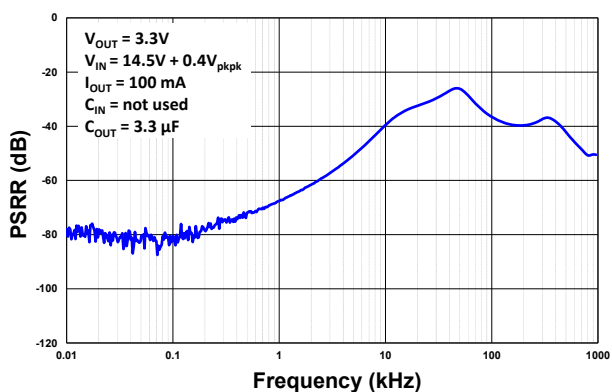


Figure 4-23. PSRR vs. Frequency (5V).

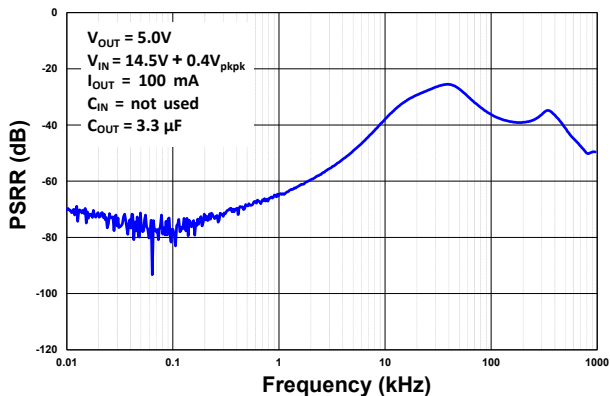


Figure 4-24. Dynamic Load Step (3.3V).

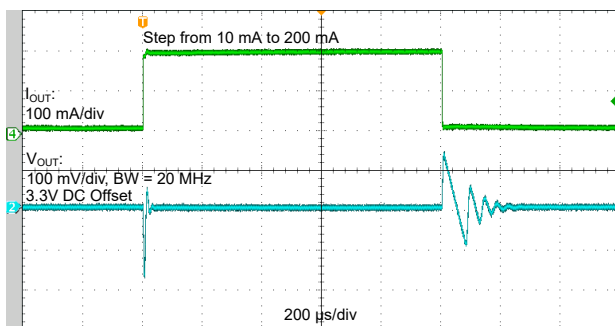


Figure 4-25. Dynamic Load Step (5V).

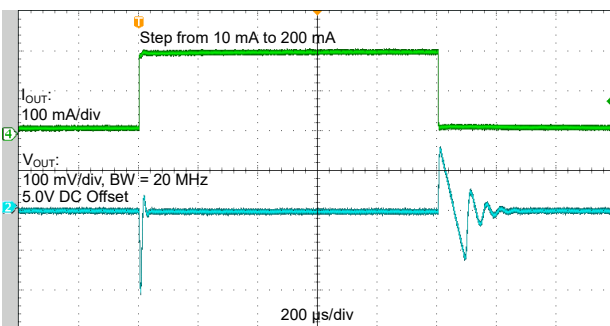


Figure 4-26. Dynamic Line Step 4.3V to 14V (3.3V).

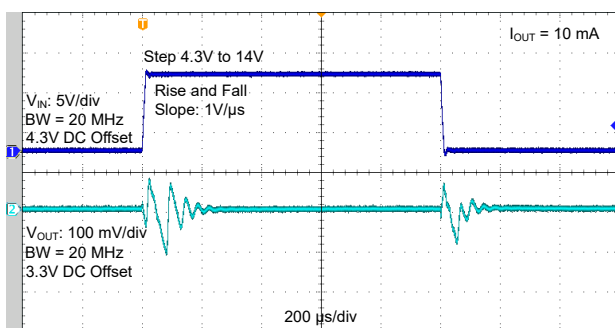


Figure 4-27. Dynamic Line Step 6V to 14V (5V).

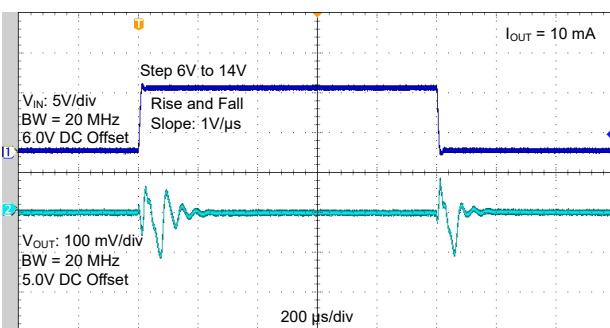


Figure 4-28. Dynamic Line Step (12V to 48V, 3.3V).

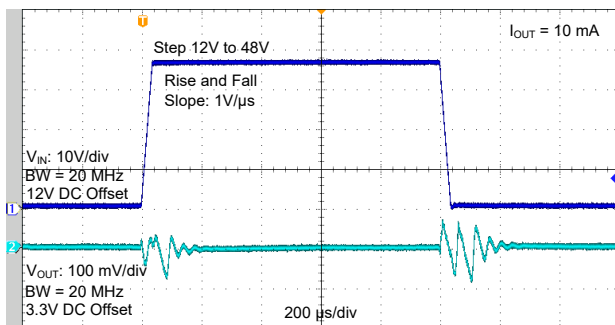


Figure 4-29. Dynamic Line Step (12V to 48V, 5V).

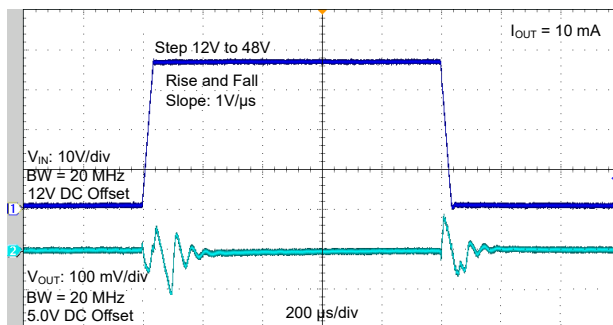


Figure 4-30. Start-up from VIN (0V to 14V, 3.3V).

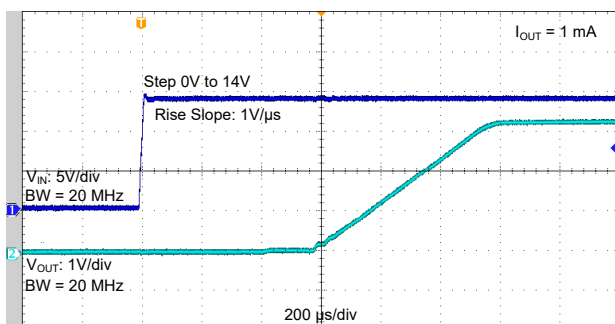


Figure 4-31. Start-up from VIN (0V to 14V, 5V).

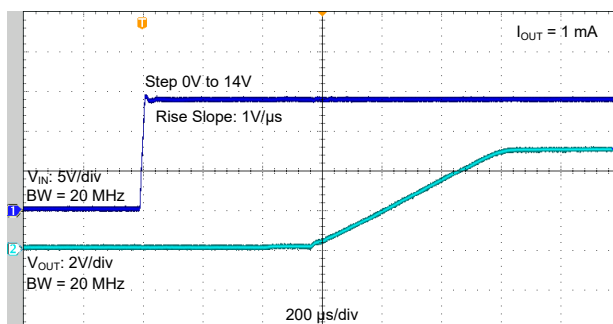


Figure 4-32. Start-up from VIN (0V to 48V, 3.3V).

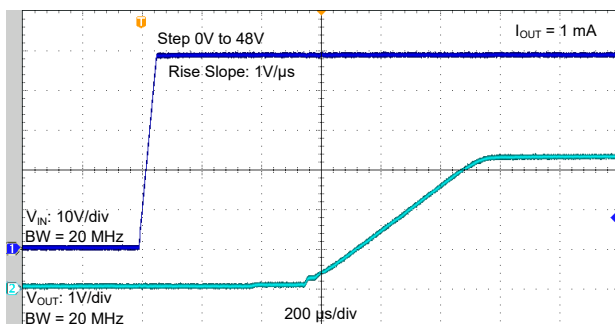


Figure 4-33. Start-up from VIN (0V to 48V, 5V).

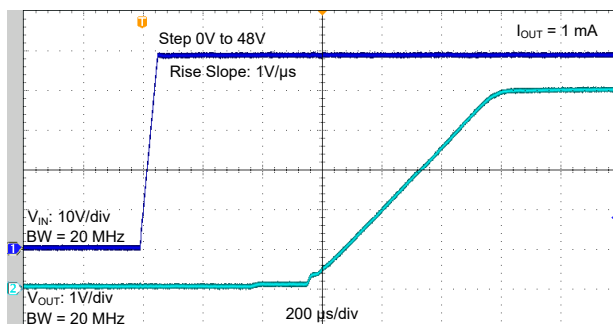
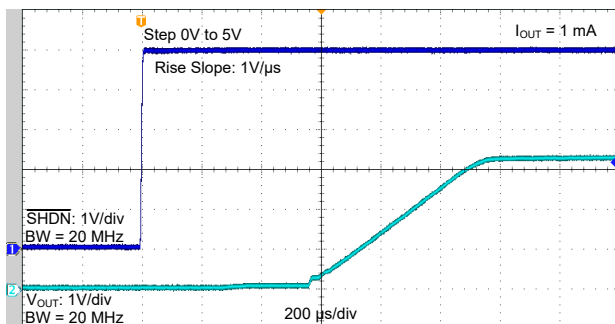
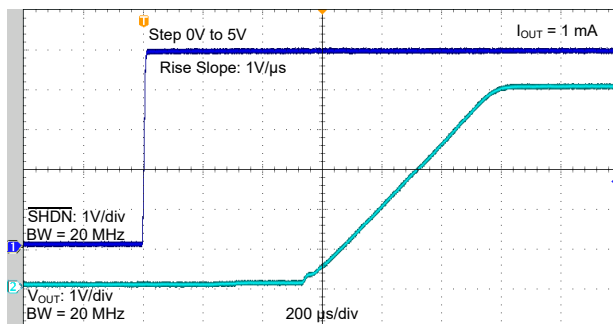
Figure 4-34. Start-up from $\overline{\text{SHDN}}$ (0V to 5V, 3.3V).Figure 4-35. Start-up from $\overline{\text{SHDN}}$ (0V to 5V, 5V).

Figure 4-36. Power Good Transitions (3.3V).

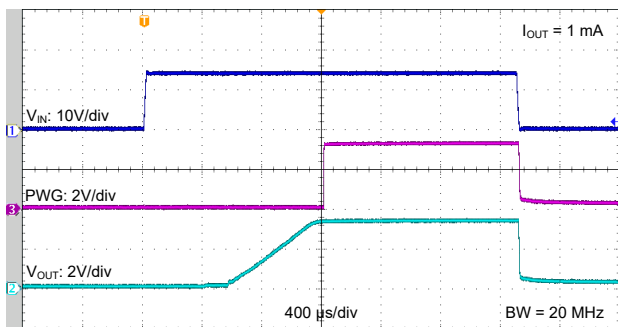
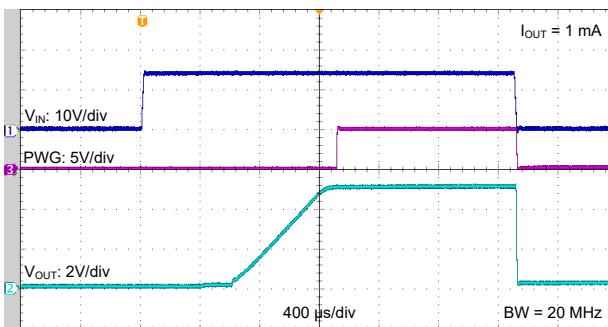


Figure 4-37. Power Good Transitions (5V).



5. Application Information

5.1. Typical Application

The MCP1781 is used for applications that require high input voltage and are prone to high transient voltages on the input (see [Typical Application Circuit](#)).

5.1.1. Power Dissipation Calculations

The internal power dissipation within the MCP1781 is a function of input voltage, output voltage, output current and quiescent current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

Equation 5-1. Internal Power Dissipation

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MAX)}) \times I_{OUT(MAX)}$$

Where:

P_{LDO} = Internal power dissipation of the LDO pass device

$V_{IN(MAX)}$ = Maximum input voltage in the application

$V_{OUT(MIN)}$ = LDO minimum output voltage

$I_{OUT(MAX)}$ = Maximum output current in the application

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1781 because of quiescent or ground current. The power dissipation as a result of ground current can be calculated by applying Equation 5-2:

Equation 5-2. Ground Current Power Dissipation

$$P_{I(GND)} = V_{IN(MAX)} \times I_{GND}$$

Where:

$P_{I(GND)}$ = Power dissipation due to the ground current of the LDO

$V_{IN(MAX)}$ = Maximum input voltage in the application

I_{GND} = Current flowing into the GND pin

The total power dissipated within the MCP1781 is the sum of the power dissipated in the LDO pass device and the ground current power dissipation term. Because of the CMOS construction, the I_{GND} for the MCP1781 is typically 85 μ A at full load. Operating at a maximum V_{IN} of 55V results in a power dissipation of 4.675 mW. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1781 is +150°C. To estimate the internal junction temperature of the MCP1781, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient (θ_{JA}) of the device. For example, the thermal resistance from junction-to-ambient for the 5-Lead SOT-223 package is estimated at 68.3°C/W.

Equation 5-3. Maximum Continuous Junction Temperature

$$T_{J(MAX)} = P_{LDO} \times \theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$ = Maximum continuous junction temperature

P_{LDO} = Total power dissipation of the device

θ_{JA} = Thermal resistance from junction-to-ambient

$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The equation below can be used to determine the package maximum internal power dissipation.

Equation 5-4. Package Maximum Internal Power Dissipation

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation of the device

$T_{J(MAX)}$ = Maximum continuous junction temperature

$T_{A(MAX)}$ = Maximum ambient temperature

θ_{JA} = Thermal resistance from junction-to-ambient

Equation 5-5. Device Junction Temperature Increase

$$T_{J(RISE)} = P_{D(MAX)} \times \theta_{JA}$$

Where:

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

$P_{D(MAX)}$ = Maximum power dissipation of the device

θ_{JA} = Thermal resistance from junction-to-ambient

Equation 5-6. Device Junction Temperature

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J = Junction temperature

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

T_A = Ambient temperature

The internal junction temperature rise is a function of internal power dissipation and of the thermal resistance from junction-to-ambient for the application. The thermal resistance from junction-to-ambient (θ_{JA}) is derived from EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction-to-ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to [Application Note AN792](#), "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application" (DS00792), for more information regarding this subject.

5.1.2. Typical Application Examples

5.1.2.1. Internal Power Dissipation

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

Equation 5-7. Power Dissipation Example

Package:

Package Type = 5-Lead SOT-223

Input Voltage:

$V_{IN} = 14V \pm 5\%$

LDO Output Voltage and Current:

$V_{OUT} = 5V$

$I_{OUT} = 100 \text{ mA}$

Maximum Ambient Temperature:

$T_{A(MAX)} = +60^{\circ}\text{C}$

Internal Power Dissipation:

$$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

$$P_{LDO} = (14.7 - 4.9) \times 100 \text{ mA}$$

$$P_{LDO} = 0.98 \text{ Watts}$$

5.1.2.2. Device Junction Temperature Rise

Equation 5-8. Device Junction Temperature Increase Example

$$T_{J(RISE)} = P_{TOTAL} \times \theta_{JA}$$

$$T_{J(RISE)} = 0.98\text{W} \times 68.3^{\circ}\text{C/W}$$

$$T_{J(RISE)} = 66.934^{\circ}\text{C}$$

5.1.2.3. Junction Temperature Estimate

Equation 5-9. Device Junction Estimate Example

$$T_J = T_{J(RISE)} + T_A$$

$$T_J = 66.934^\circ\text{C} + 60^\circ\text{C}$$

$$T_{J(RISE)} = 126.934^\circ\text{C}$$

5.1.2.4. Maximum Package Power

Dissipation at +60°C Ambient Temperature.

Equation 5-10. Maximum Allowable Dissipation at +60°C Ambient Temperature

5-Lead SOT-223 ($\theta_{JA} = 68.3^\circ\text{C}/\text{W}$):

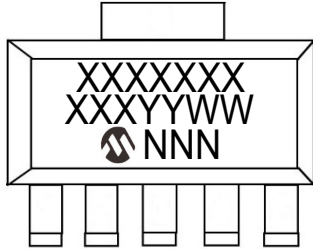
$$P_{D(MAX)} = \frac{150^\circ\text{C} - 60^\circ\text{C}}{68.3^\circ\text{C}/\text{W}}$$

$$P_{D(MAX)} = 1.317\text{W}$$

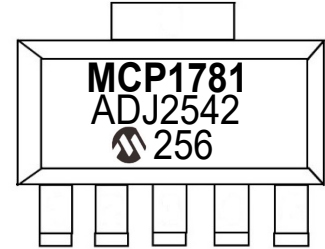
6. Package Information

6.1. Package Marking Information

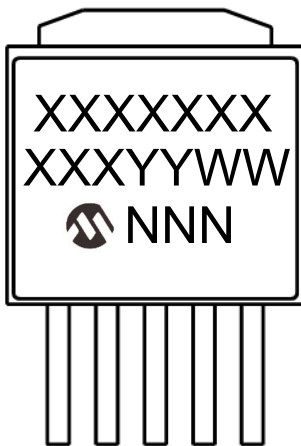
5-Pin SOT-223:



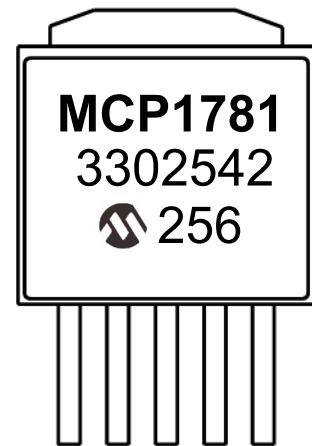
Example:



5-Pin TO-252:



Example:

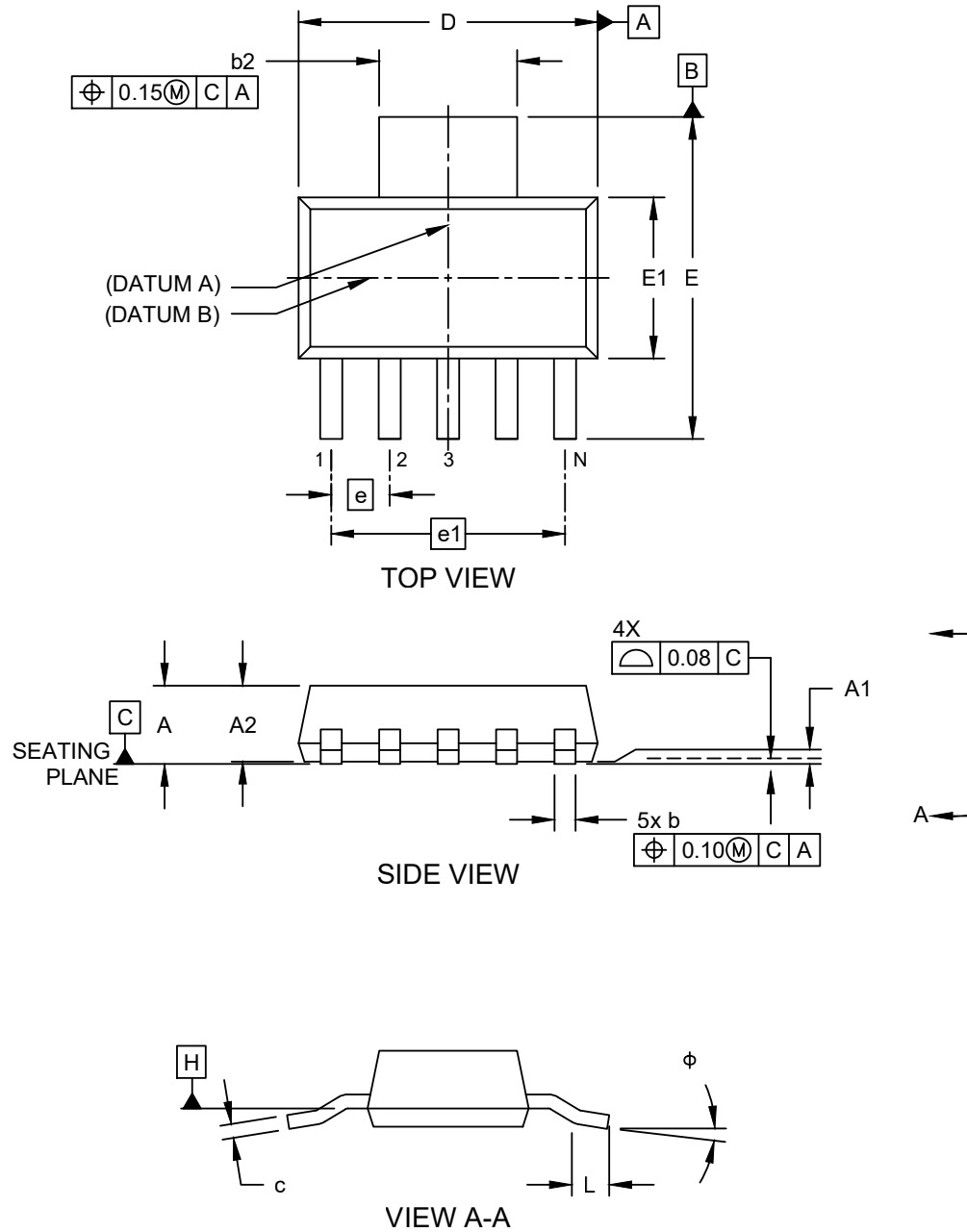


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.	

6.2. Package Outline Drawings

5-Lead Plastic Small Outline Transistor (N7X) [SOT-223]

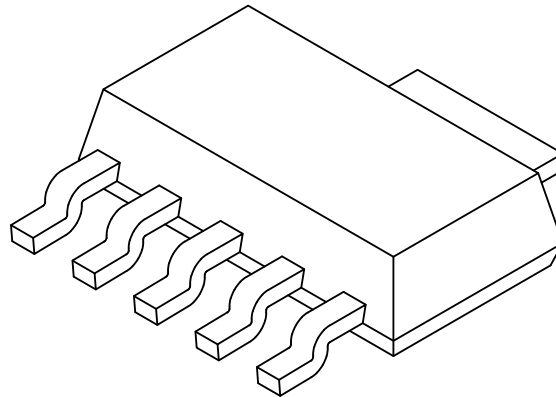
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-00137-N7X Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (N7X) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	5		
Lead Pitch	e	1.27 BSC		
Outside lead pitch	e1	5.08 BSC		
Overall Height	A	-	-	1.80
Standoff	A1	0.02	0.06	0.10
Molded Package Height	A2	1.55	1.60	1.65
Overall Width	E	6.86	7.00	7.26
Molded Package Width	E1	3.45	3.50	3.55
Overall Length	D	6.45	6.50	6.55
Lead Thickness	c	0.24	0.28	0.32
Lead Width	b	0.41	0.46	0.51
Tab Lead Width	b2	2.95	3.00	3.05
Foot Length	L	0.91	-	-
Lead Angle	ϕ	0°	-	10°

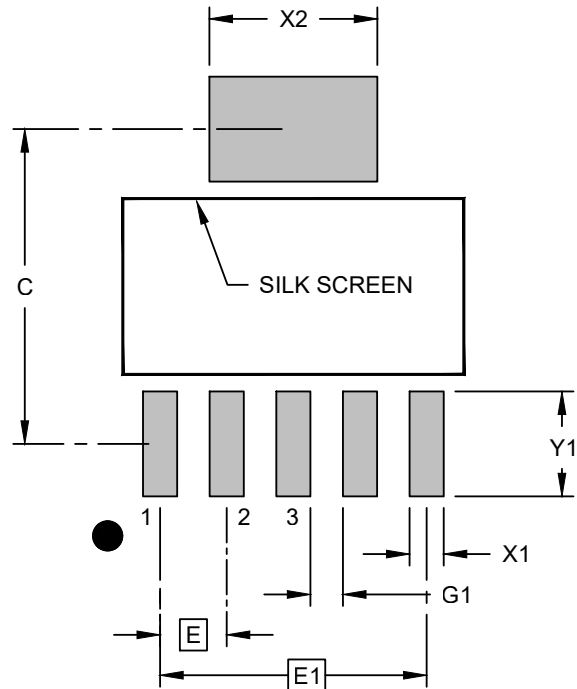
Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash protrusions shall not exceed 0.127mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00137-N7X Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (N7X) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pitch	E1	5.08 BSC		
Contact Pad Spacing	C		6.10	
Contact Pad Width (X5)	X1			0.65
Contact Pad Width	X2			3.20
Contact Pad Length (X6)	Y1			1.90
Distance Between Pads (X4)	G1	0.62		

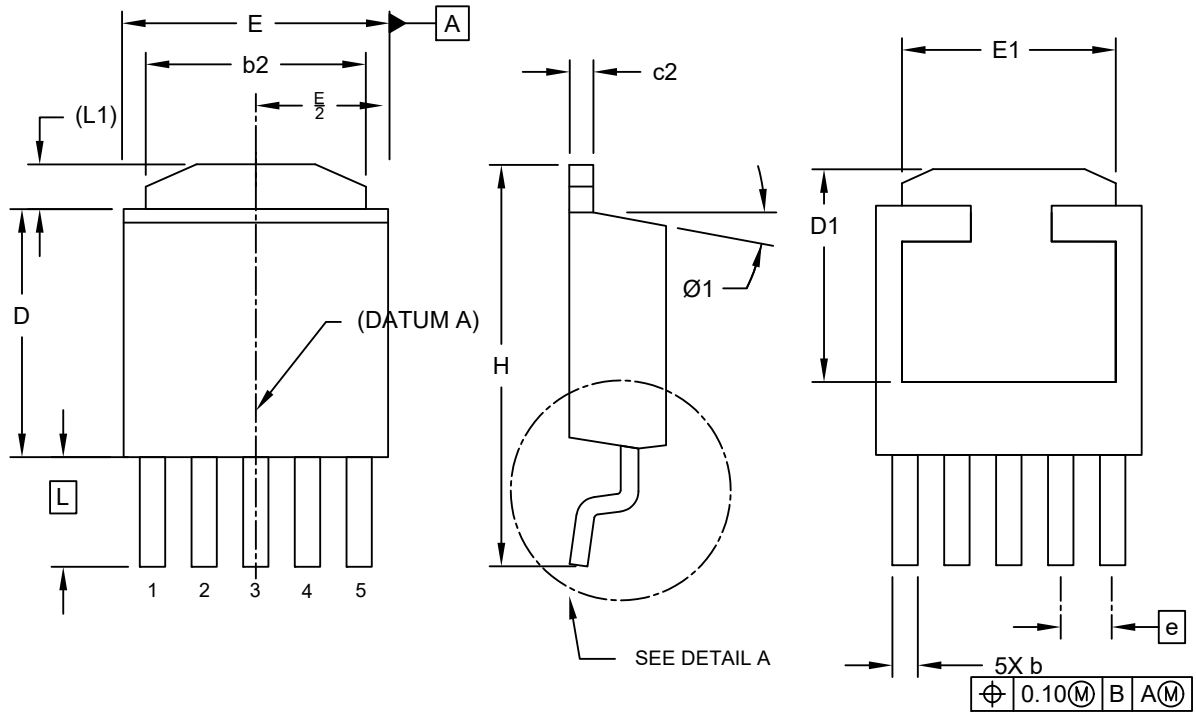
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during the reflow process.

Microchip Technology Drawing C04-02137-N7X Rev E

5-Lead Transistor Outline (9EA) - [TO-252] Option "A"

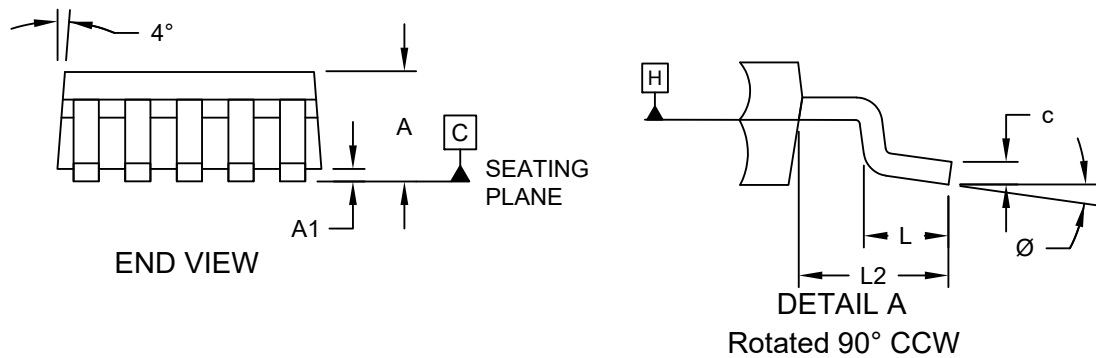
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



TOP VIEW

SIDE VIEW

BOTTOM VIEW



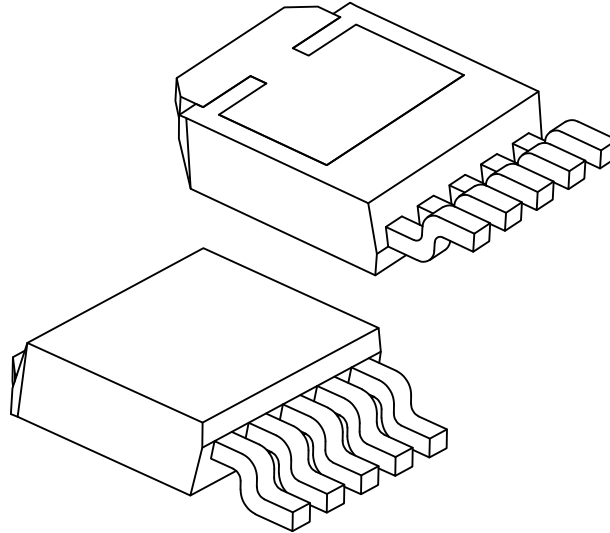
END VIEW

DETAIL A
Rotated 90° CCW

Microchip Technology Drawing C04-1168 Rev A Sheet 1 of 2

5-Lead Transistor Outline (9EA) - [TO-252] Option "A"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits		MILLIMETERS		
		Min	Nom	Max
Number of Leads	N	5		
Pitch	e	1.27 BSC		
Overall Height	A	2.18	–	2.38
Seating Plane Height	A1	–	–	0.127
Lead Width	b	0.508	–	0.771
Thermal Pad Width	b2	4.95	–	5.46
Lead Thickness	c	0.46	–	0.61
Thermal Pad Thickness	c2	0.46	–	0.89
Molded Body Length	D	5.97	–	6.22
Thermal Pad Length	D1	5.21	–	–
Total Width	E	6.35	–	6.73
Thermal Pad Width	E1	4.32	–	–
Overall Length	H	9.39	–	10.41
Foot Length	L	1.39	–	1.78
Tab Length	L1	1.067 REF		
Lead Length	L2	2.74 BSC		
Foot Angle	θ	0°	–	10°
Mold Draft Angle	θ1	0°	–	15°

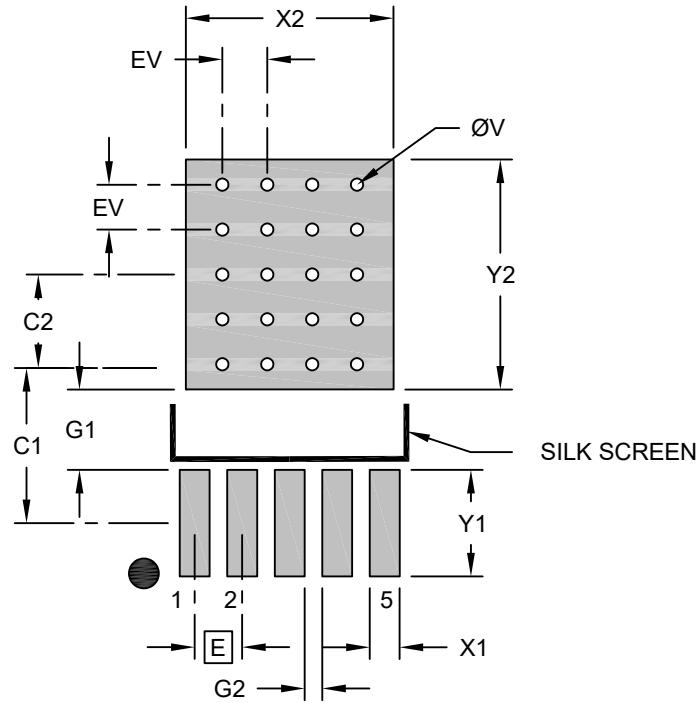
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1168 Rev A Sheet 2 of 2

5-Lead Transistor Outline (9EA) - [TO-252] Option "A"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Center Pad Width	X2			5.55
Center Pad Length	Y2			6.15
Contact Pad Spacing	C1		4.15	
Contact Pad Spacing	C2		2.50	
Contact Pad Width (X5)	X1			0.80
Contact Pad Length (X5)	Y1			2.85
Contact Pad to Center Pad (X5)	G1	2.15		
Contact Pad to Contact Pad (X4)	G2	0.47		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3168 Rev A

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: <https://www.microchip.com/en-us/about/contact-us>.

<u>PART NO.</u>	[T]	-XX(X)	XX	X	/XX(X)	XXX
Device	Tape and Reel ⁽¹⁾	Voltage	Feature Code	Temperature Range	Package	Qualification

Device:	MCP1781: 200 mA High-Voltage Automotive LDO	
Media Type⁽¹⁾:	(blank)	= Tube (80/Tube – 9EA; 1/Tube – DC)
	T	= Tape and Reel (2,500/Reel – 9EA; 4,000/Reel – DC)
Voltage:	33	= 3.3V
	50	= 5.0V
Feature Code:	02	= Fixed Voltage
Temperature Range:	H	= –40°C to +150°C (High)
Package:	9EA	= 5-Pin TO-252 Transistor Outline (Code: 9EA)
	DC	= 5-Pin SOT-223 Plastic Small Outline Transistor (Code: N7X)
Qualification:	(blank)	= Standard Part
	VAO	= AEC-Q100 Automotive Qualified

Examples:

- MCP1781-3302H/9EA: 200 mA High-Voltage Automotive LDO, Tube, 3.3V Fixed Output Voltage, High Temperature Range, TO-252 Package
- MCP1781T-5002H/DC: 200 mA High-Voltage Automotive LDO, Tape and Reel, 5.0V Fixed Output Voltage, High Temperature Range, SOT-223 Package
- MCP1781-3302H/DCVAO: 200 mA High-Voltage Automotive LDO, Tube, 3.3V Fixed Output Voltage, High Temperature Range, SOT-223 Package, AEC-Q100 Automotive Qualified
- MCP1781-5002H/9EAVAO: 200 mA High-Voltage Automotive LDO, Tube, 5.0V Fixed Output Voltage, High Temperature Range, TO-252 Package, AEC-Q100 Automotive Qualified

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legal-information/microchip-trademarks>.

ISBN: 979-8-3371-2073-7

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.